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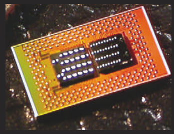
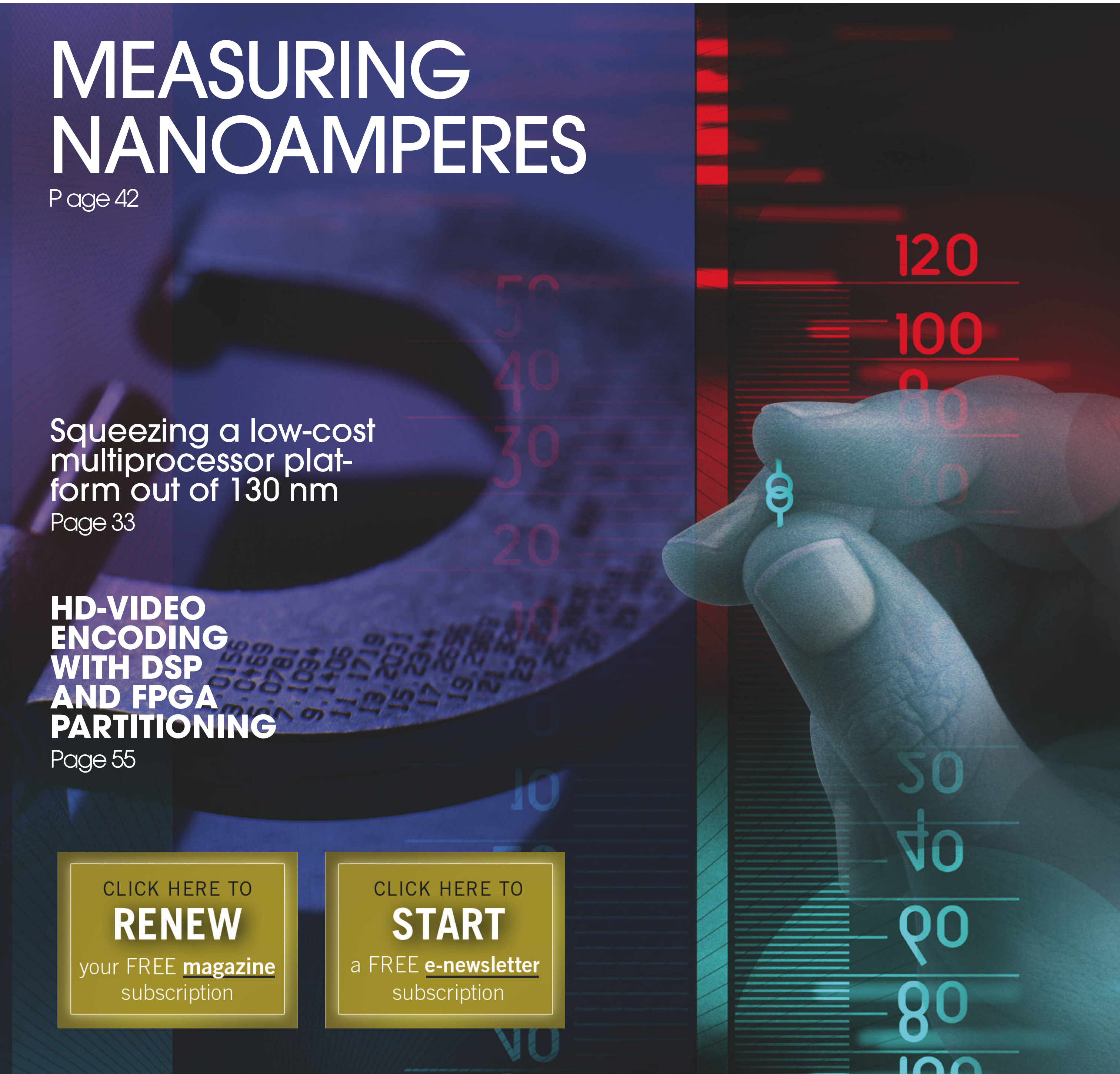




MEASURING NANOAMPERES

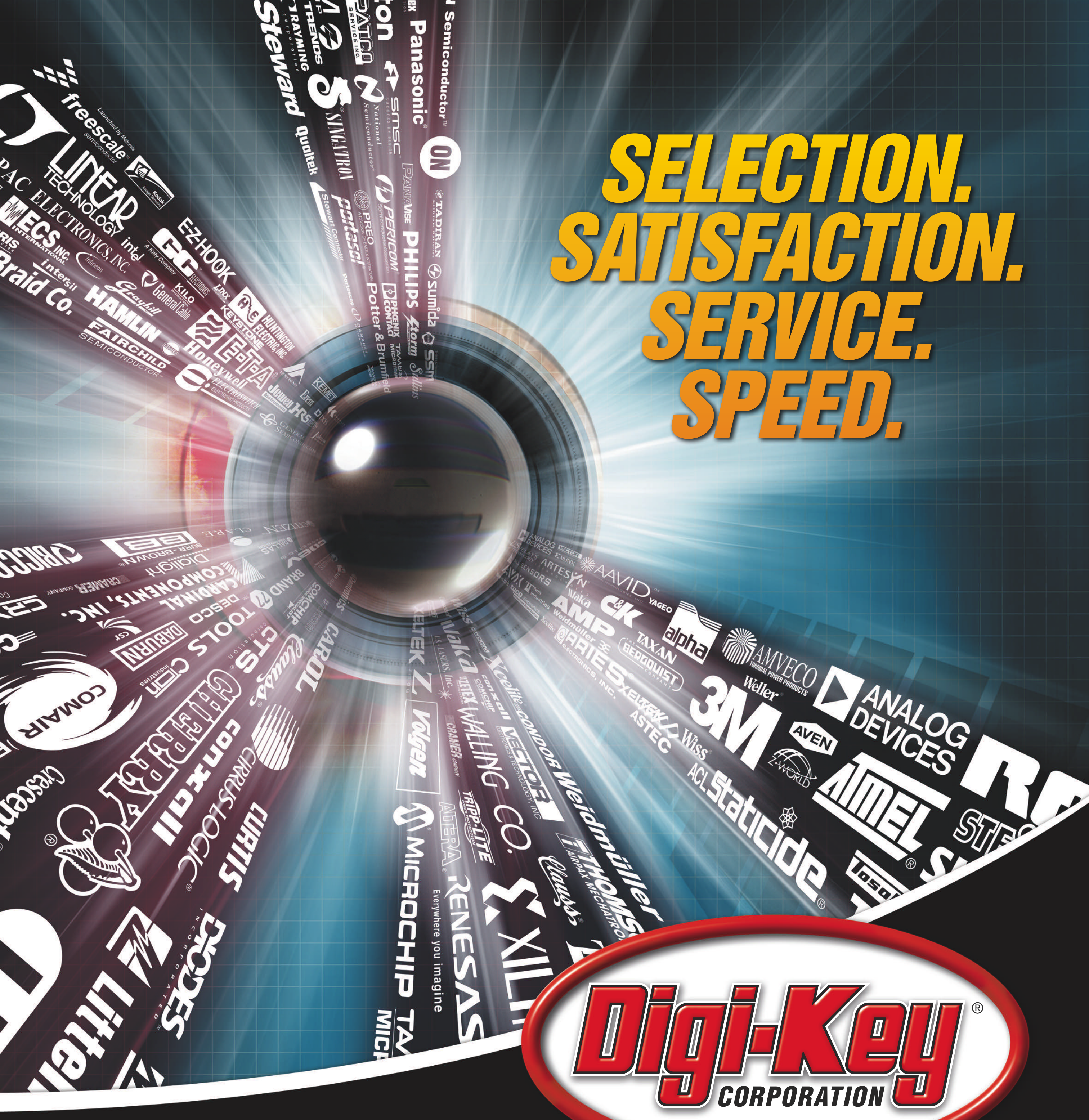
P age 42

Squeezing a low-cost multiprocessor platform out of 130 nm

Page 33

HD-VIDEO ENCODING WITH DSP AND FPGA PARTITIONING

Page 55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EDN contents

4.26.07

HD-video encoding with DSP and FPGA partitioning

55 Implementing a scalable video-encoding architecture that includes DSPs and, when necessary, FPGAs as coprocessors to offload certain tasks satisfies even the most demanding video applications.

by Cheng Peng, PhD, and Thanh Tran, PhD, Texas Instruments

Measuring nanoamperes

42 Measuring low currents can be tricky. Clever analog-design techniques and the right parts and equipment can help.

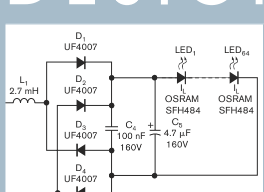
by Paul Rako, Technical Editor

Squeezing a low-cost multiprocessor platform out of 130 nm

33 LSI's Zevio project shows that success in consumer electronics does not always mean implementing the fastest SOC in the latest and greatest process technology.

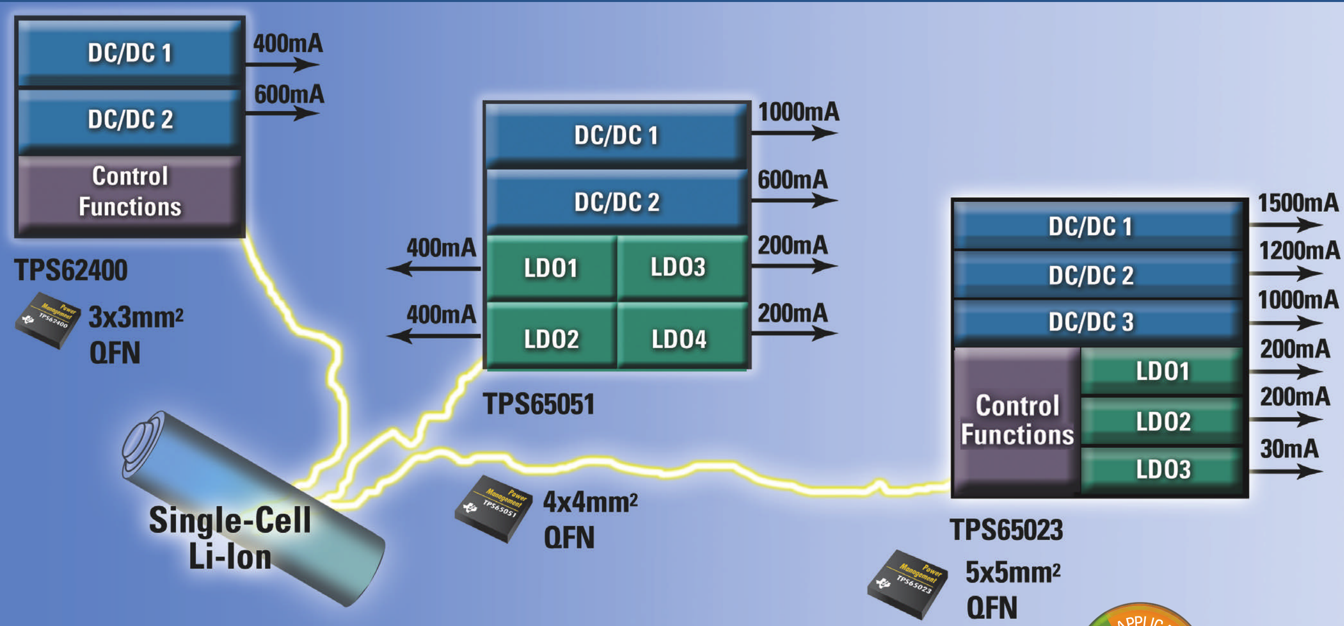
by Michael Santarini, Senior Editor

DESIGNIDEAS



High Integration = Smaller Solution Size

Multi-Channel Power Management Units for Single Cell Li-Ion Systems



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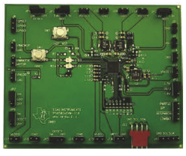
TPS65020	6	–	3	1.5MHz	3	I²C	2.5 to 6.0	6x6mm²	TI DM320, Marvell PXA270	$3.75
TPS65023	6	–	3	1.5MHz	3	I²C	2.5 to 6.0	5x5mm²	TI DaVinci™ Technology	$3.85
TPS65050	6	–	2	2.25MHz	4	–	2.5 to 6.0	4x4mm²	Samsung S3C241x	$2.75
TPS65051	6	–	2	2.25MHz	4	–	2.5 to 6.0	4x4mm²	TI OMAP850, Marvell PXA255	$2.75
TPS65820	12	Yes	3	1.5MHz	7	I²C	3.0 to 18	7x7mm²	General Purpose	$6.50

** Suggested resale price in U.S. dollars in quantities of 1,000.*



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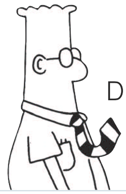

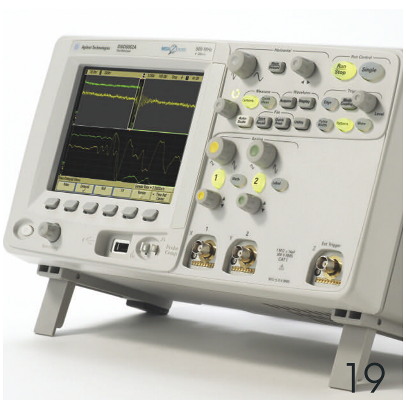

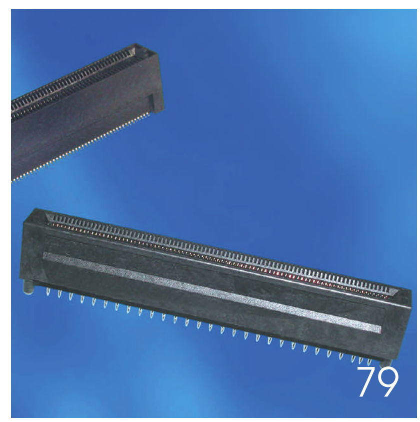

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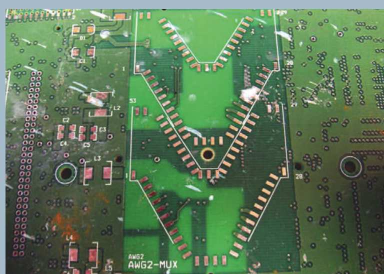

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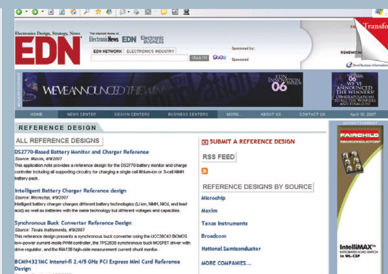

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BY MATTHEW MILLER, EDITOR IN CHIEF, EDN.COM

10 reasons to visit EDN.com

Please allow me to give you 10 reasons to visit the new EDN.com. I know you're busy, so unlike David Letterman, I'll start with No. 1.

1 Design Centers: Many sites choose to organize information based on product categories, markets, or technology trends. But, in redesigning EDN.com we thought about engineers and how they work. We thought about how an analog engineer, for example, has different interests from a communications-system or IC designer. Each requires different information, uses different terminology, and even has a different mindset.

Based on this engineer-centric way of thinking, *EDN* developed a set of Design Centers focusing on distinct engineering disciplines, such as analog design, IC design, consumer electronics, processor-based design, and power management.

Each Design Center delivers not only in-depth technical articles, product news, and opinions from *EDN*'s editors, but also a wide range of information from outside our walls, such as contributed how-to articles, details on reference designs, and information on key technical conferences. And, because all of that information is germane to one engineering discipline, the Design Centers also perform a critical function in this information-soaked age: They filter, so that you needn't waste your time digging through irrelevant stuff.

We've unleashed one of our editors—most of whom are EEs—to build up each Center. They'll perform this job through their own articles; by sparking discussions in their blogs; and by procuring useful, hype-free content from relevant vendors. They'll even gather video clips and other multimedia when that type of data can help to explain a complex concept.

2 A 3-D view: EDN.com now includes breaking-news coverage from the editors of *Electronic News*, plus strategy and management insights from the editors of *Electronic Business*. We don't ever skimp on technical content, but, in this increasingly demanding industry, we hope that you'll find these additional facets of coverage useful, too.

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9 Better design: This point is subjective, but we think you'll agree that the new EDN.com is faster to navigate (with handy pulldown menus) and easier on the eyes (with a wider format and overall larger fonts).

10 Resource Center: *EDN*'s Resource Center—visible toward the bottom of the home page and some of the Design Center pages—contains paid listings from vendors. But, in focus groups and surveys, you've told us that you need such information to do your job, and our advertisers use the Resource Center to provide useful items, such as white papers and design guides.

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Reed Electronics Group

RAQ's

Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Breadboarding With Surface Mount ICs
Too small, or not too small? That is the question...

Q. *How do I build breadboards with tiny surface mount (SM) ICs?*

A. Very carefully — with a printed circuit board (PCB) IC carrier, a solder-well tip to your soldering iron, plenty of flux and a powerful magnifier.

It is seminar time in Europe. Every couple of years, Analog Devices gives about a hundred seminars around the world on topics related to one of our product lines. The current topic is high speed systems. Over six months I shall be giving it in over thirty countries, mostly European, and eating a lot of plastic airline meals as I travel to do so.

A good seminar is a dramatic performance as well as a technical exposition. Seminar speakers should encourage questions to promote audience participation — and at times the questions come fast and furious. Surprisingly, one of the most common questions is not about circuit design — it is about handling tiny modern IC packages in a development laboratory environment in a way that allows major circuit changes to be made without damaging the IC. Breadboarding with dual inline packages (DIPs) was easy, but is tough with small outline ICs (SOICs) and a nightmare with smaller packages having lead pitches of 0.025" or less.

There is a solution. If we build small PC boards with pads and tracks fitting these small packages, but leading to relative large (0.1" × 0.2" [2.5 mm × 5 mm]) pads around their edges, we can mount the ICs on the PCBs and then breadboard with conveniently-sized leaded components. If the underside of the PCB is a ground plane, we can decouple the IC to it and use it to mount the PCB to a copper-clad breadboard (using solder and a HOT soldering iron).

This does leave the problem of mounting the IC on its PCB carrier. In fact, a thermostatic soldering iron with a solder-well tip and plenty of flux makes the task of mounting small surface-mount ICs less difficult than it seems. Two leads are soldered down with a fine pointed iron to fix the device in position, and then all the leads are well coated with flux. The "well" in the soldering iron is filled, but not overfilled, with solder and is drawn across the leads on one side of the IC. This solders the leads and, if done carefully, does not short-circuit them to each other. The operation is repeated on each leaded side of the IC, then the board is inspected for short-circuits or unmade joints.

The soldering can be done under a bench magnifier or with high power (5-6 dioptre) reading glasses. The links describe the boards and the mounting technique in more detail.

To learn more about breadboards,
Go to: http://rbi.ims.ca/5387-101

Have a question involving a perplexing or unusual analog problem? Submit your question to:

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Powering Portable Media Players (PMP) with Innovative Solutions [Part 1 of 2]

Application Note AN-1608

Dipak Patel, Applications Manager

In the past, when system designers were handed a project, they basically purchased off-the-shelf discrete power solutions from the various vendors. The list of issues the power designer must consider has greatly increased as power systems have become more complicated. Some of the key areas where these new design challenges exist are:

- Multiple outputs due to feature-rich devices, LDOs, Bucks, battery chargers; overall more control of the system is required to obtain better efficiencies during battery operation.
- To ensure stable multiple voltage supplies to the host processor, IC systems now require increased flexibility, programmability, and power sequencing to allow for powering down unused power functions when left unused.
- Finding an easy to implement, correct and easy-to-use power management solution can become a critical part of rapid system development and improved cycle time-to-market.
- By having a high level of integration in such a PMIC reduces overall system cost and size constraint significantly when compared to equivalent discrete solutions.
- Extending battery life now requires higher efficiencies and DVS (Dynamic Voltage Scaling) to reduce overall power consumption.

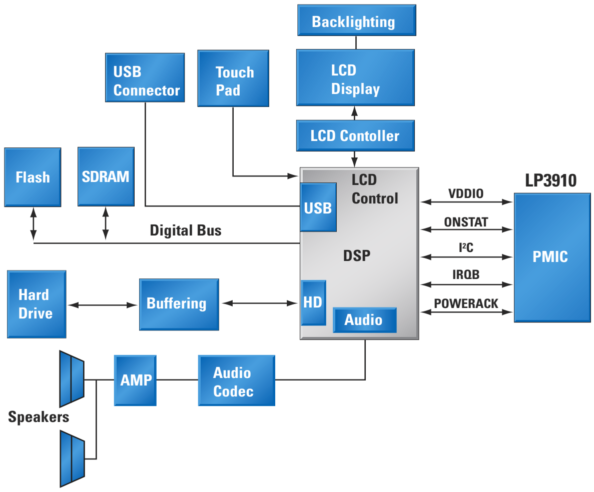

Figure 1. Portable Media System Level Diagram

The system diagram in **Figure 1** details the many power requirements of a typical personal media player (PMP). Using smart power control in your design can yield improved performance in many areas including:

- Digital signal processor
- Hard drive for storage of the downloaded media
- Touch pad to select software driven functions of the media player
- LCD display
- Audio amplifier
- Audio Codec
- Flash memory used to store the operating system; upon system boot up of the DSP, the bootloader instructs the DSP to download the OS image from Flash to the SDRAM
- SDRAM storage of the OS image, SDRAM has faster access time than flash so the DSP can access information quickly
- USB interface to download music content from a computer

Many of these challenges can be seen when designing in power requirements for PMPs. These devices have a multitude of constraints and unique needs that can be better handled when using smart, programmable power controllers. **Part 1** of this article includes details of the design specifics on powering the main subsystems. In **Part 1** we'll also review how the integration of various power and control functions into a common IC can solve system issues such as: powering subsystems, digital application/peripheral, audio amplifier block, DSP (I/O, Core), and memory, hard disk drive, and LCD backlight display.

In **Part 2** we'll review more key features that affect design and power management such as: battery charging and monitoring, battery charger linear charger, smart control parameters, power prioritization routing, power sequencing, soft-start, and communication between the PMIC and the DSP.

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Powering the Digital Application / Peripheral

Typically Low Drop Out (LDO) regulators are used to power digital peripherals. Voltages are usually 1.2V to 3.3V with a current requirement of 150 mA. Good external output filtering is also required. Digital loads require LDOs to have good load transient response to keep the output voltage in regulation.

Powering the Audio Amplifier Block

An LDO is required in this application as the noise generated from a switch mode supply will introduce excessive noise into sensitive analog circuits. Here, the important parameter to consider is the Power Supply Rejection Ratio (PSRR). If transients on the power supply line are not suppressed, harmonics will appear at the speaker output. Attention to good output filtering and PCB layout is important.

Powering the DSP (I/O, Core), and Memory

Typically, magnetic buck switching regulators are used to power the DSP and memory due to the high load demand and high efficiency requirement.

Buck 1 and 2 are high efficiency synchronous FET (low rds) switching regulators. A multiphase switching scheme has been implemented such that NFET, and PFET of buck 1 are turned on/off at fixed phase intervals in time which are different to that of buck 2 using counter logic. This reduces the overall demand from the main DC source or battery.

The output voltages can be changed via I^2C if dynamic voltage scaling is required. The concept is to dynamically scale the output voltage up or down based on the load demand at that moment in order to maximize the overall system power saving. For example, when the DSP is running in a mode where it is reading or writing large amounts of data to memory or doing intensive numerical calculations where the power needs to change dramatically. By using the I^2C the voltages can be changed. Once the function is completed the DSP informs the PMIC to go back to the lower voltage setting. This type of power management technique increases the longevity of the battery.

The bucks operate at 2 MHz which means the physical dimensions of the external inductor are considerably reduced. Below is a typical efficiency plot for a magnetic switching buck regulator.

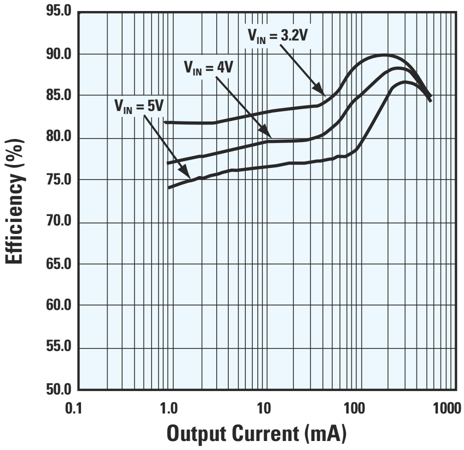

Figure 2. Typical Efficiency vs I_{OUT} for a 2 MHz Magnetic Buck Switching Regulator

Powering the Hard Disk Drive

The Buck-Boost is required when extending the device runtime 3.3V for the hard drive during battery operation. This voltage is lower than the maximum battery of 4.2V and higher that the minimum battery of 2.8V. In addition it needs to supply a peak current initially of about 500 mA for the motor on the hard drive spindle to turn. During read write cycles to the hard drive the current averages about 200 mA.

Powering the LCD Backlight Display

A Boost circuit is required to power the LCD backlight display. This is required to produce a large voltage which tends to be greater than the supply voltage for the lighting supply to the LCD display. A magnetic or switched capacitor boost regulator can be used as an LED backlight driver. ■

To read Part 2 of "Powering Portable Media Players (PMP) with Innovative Solutions " go to
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EDITED BY FRAN GRANVILLE

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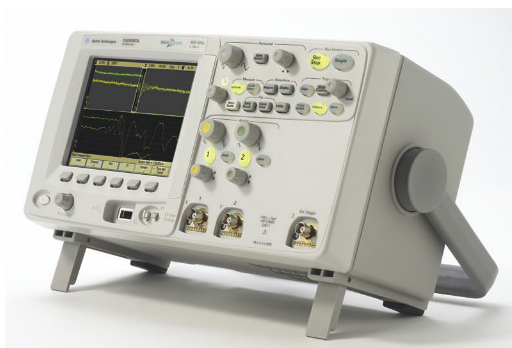
INNOVATIONS & INNOVATORS

Popularly priced DSOs aim to outsell market leader

According to Agilent Technologies, Tektronix's (www.tektronix.com) lunchbox-sized TDS3000 series remains the largest-selling oscilloscope family based on the number of units sold. Because of the TDS3000s' low prices, however, the series is probably not the market leader in revenues. Nevertheless, Agilent aims to wrest the unit-sales crown from the TDS3000s. To do so, Agilent has introduced the 5000 series. The 5000s' cases are about the same size as those of the TDS3000s. The modest-sized screens are equal in size, although Agilent says that, by enabling users to switch off the on-screen display of soft-key legends, the 5000s can use more of the LCD to display waveforms. Hence, says Agilent, its units can present a bigger picture of what you buy a scope to see: waveforms.



Because of their deep memory, fast waveform-update rate, and high-definition display system, 5000-series oscilloscopes, such as this two-channel unit, enable engineers to quickly investigate signal anomalies.

Architecturally, the two series differ significantly. Tektronix based the TDS3000 family on a FISO (fast-in/slow-out) architecture that has served Tek's customers well for nearly a generation. FISO scopes use an IC analog memory—a form of CCD (charge-coupled device)—to rapidly store analog-waveform samples and then more slowly deliver them to a modest-speed ADC. Although it believes that—if it wanted to—Tek could extend FISO-memory depth well beyond the TDS3000s' 10,000 samples/channel, Agilent believes that, within the TDS3000-series price constraints, Tek cannot extend its FISO memory depth to the megasample depth of the 5000 series' patented MegaZoom architecture or the memory depths of most of Tek's own higher priced scopes.

The six members of Agilent's 5000 series include two- and four-channel units with analog bandwidths of 100, 300, and 500 MHz. The maximum sampling rate of the 100- and 300-MHz units is 2G samples/sec/channel, and that of the 500-MHz units is 4G samples/sec/channel. All units offer maximum memory depth of 1M sample/channel—100 times that of the TDS3000s. Prices for the 5000s range from $4050 to $9995.

The maximum sampling rate is never less than 6.67 times the analog bandwidth, a ratio that is more than adequate for waveform reconstruction. The scopes always interpolate between sampled-data points. Therefore, under conditions that cause competitive instruments to display collections of dots that can be difficult to interpret—especially when a scope is displaying data from multiple channels—the 5000s connect the dots to display waveforms that look like waveforms. Moreover, the 1024×768-pixel color displays support 256 intensity levels and update at 100,000 waveforms/sec, which Agilent says is 25 times the rate of the fastest-updating competitive scopes.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com.

FEEDBACK LOOP

"I can't hear any of these effects, so I guess I cannot be noble-born. My parents will be saddened by this loss of blue blood in the family. Must dash, sorry. I'm just heading off to the store to get my pole-aligned, hermetically sealed, carbon-fiber-shrouded ac-line filters."

—James King, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6418215. Add your comments.

Synopsys tools tackle verification progress

When have you done enough verification? That's the age-old question Synopsys is attempting to answer with three new additions to its IC-verification lineup. In 2005, Synopsys and ARM (www.arm.com) introduced *Verification Methodology Manual for SystemVerilog*, by Janick Bergeron, Eduard Cerny, Alan Hunter, and Andrew Nightingale (ISBN 978-0-387-25538-5, Springer, 2006). The book outlines how to introduce assertions into advanced IC-verification-tool flows. Now, the company is taking that knowledge a step further by incorporating tools that help verification teams create and monitor verification methodologies and more easily incorporate assertion-based verification into flows.

The three new VMM (*Verification Methodology Manual*) applications, which hook to the company's VCS (Verilog Compiled Simulator) environment, are VMM Planner, VMM Applications, and VMM Automation. "The biggest challenges in verification are determining how much progress has been made, being able to measure that progress, and, based on that measurement, predicting how close verification engineers are to closure while guaranteeing quality for the design they are verifying," says Swami Venkat, director of product marketing for RTL (register-transfer-level) verification at Synopsys.

Traditionally, design teams use a spreadsheet to create verification plans and write scripts to extract data from non-machine-executable simulation-log files to monitor verification progress. Traditionally, this method has been difficult to maintain, and it relies on every design team member's diligence. So, Synopsys has figured out a way to automatically tie in much of that verification-data monitoring to its verification environment with VMM Planner, which allows verification managers to capture, track, and measure verification progress. "VMM makes planning more definable, and the data being used for planning is machine-executable," says Venkat. The tool captures data from verification tools using spreadsheet formats and then rolls up a variety of verification results, such as code and functional coverage, formal and dynamic assertions, and test pass/fail data, into an annotated plan. The tool hierarchically organizes verification projects and allows users to track source files; code, assertion, and state-machine coverage; lines of code that have changed; and pass/fail data and bug tracking. "Depending on what a team feels is important for it to track, it can define that factor as a metric, and VMM Planner will allow the team to track progress against that metric," says Venkat.

> "Synopsys has figured out a way to automatically tie in much of that verification-data monitoring to its verification environment.

With VMM Applications, Synopsys attempts to help designers more easily and more quickly create testbenches. The company has built macroblocks of high-level test functions from basic SystemVerilog elements in its VMM-standard library. The company is rolling out the first version of VMM Applications with macroblocks for the register-abstraction layer to help verification engineers verify chip registers with tests that the tool automatically generates. The tool also has macros for the abstraction layer to help users configure VMM testbenches to mixed simulation environments, hardware-assisted verification environments, or both. VMM Applications users will also be able to create reusable verification subsystems, and the tool features a memory-allocation manager that checks designs for memory-buffer content and address bugs.

VMM Automation features the VMM SystemC and VMM Compliance Checker applications. VMM SystemC acts as a higher performance interface between VMM SystemVerilog testbenches and SystemC reference models, and VMM Compliance Checker checks that verification environments comply with the rules and guidelines of *Verification Methodology Manual* for SystemVerilog, which helps verification teams further increase their chances of speeding through verification. VMM Planner and VMM Applications are available now in beta, and Synopsys hopes to have VMM Automation tools ready over the next 12 to 24 months. The tools are free with the VCS Simulator or the Pioneer testbench tools.

—by Michael Santarini

▷**Synopsys Inc**, www.synopsys.com.

DILBERT By Scott Adams

FEEDBACK LOOP

"Marv, use the $200 bucks to buy a new garage door opener. :)."

—Chuck Adams, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6421388. Add your comments.

Sigrity introduces cost-savvy power-decoupling-capacitor tool for PCB and package design

One of the longest running problems in PCB (printed-circuit-board) design has been trying to figure how much decoupling capacitance you need for your design. PCB engineers often use too much decoupling capacitance to ensure that their designs will achieve power stability requirements of their system and still meet performance goals. But each decoupling capacitor adds extra cost to the design, and typical designs have a lot of unnecessary capacitance.

Addressing this problem, Sigrity Inc recently introduced a smart decoupling-capacitance tool that helps users place just enough capacitance in their designs to reduce costs and still meet performance goals. The company's new OptimizePI targets PCB- and package-decoupling capacitance. The tool's inputs are a user-customizable library and the layout of the design. Users select the best candidates for their designs from the library and then direct the tool to analyze the layout. "The tool selects at each location what is the best capacitor they should choose from the library," says Jiayuan Fang, president of Sigrity. "The tool does a large-scale statistical analysis and automatically tries a lot of schemes. The tool then automatically places the appropriate decoupling capacitance where it is needed on the board based on performance and cost constraints. Given target performance, this tool will automatically find what the lowest cost is."

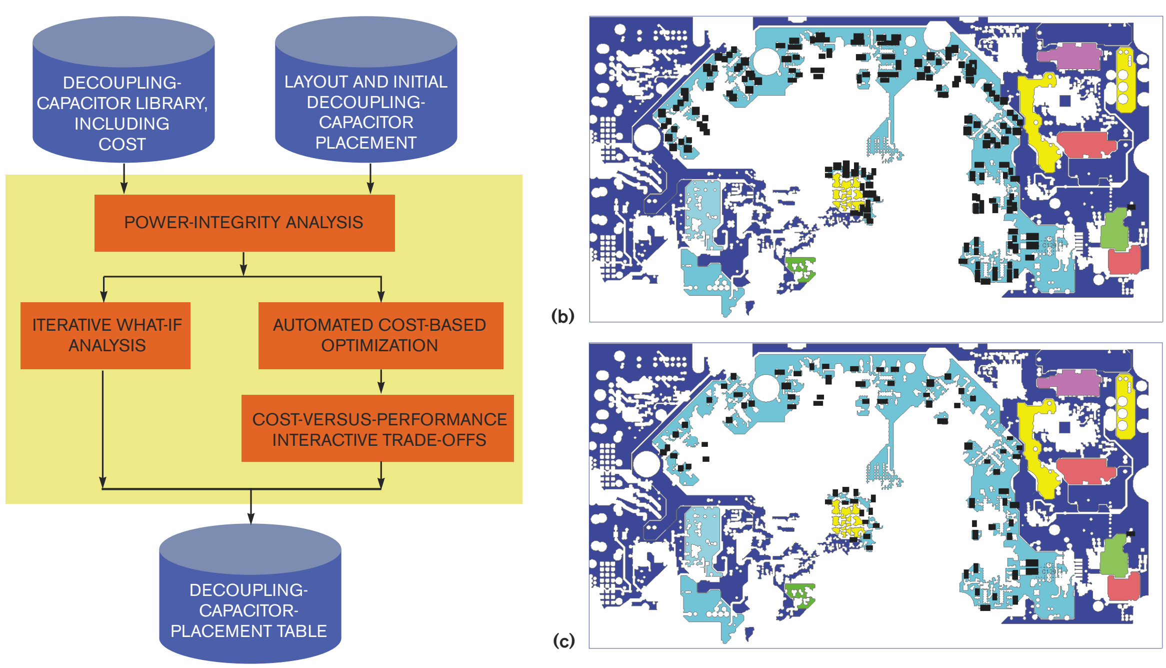
The tool has a what-if capability that allows users to test capacitors for the right balance of performance and cost. "It adds a new dimension of automation because you are able to stabilize your power-delivery system and achieve a performance level at a much reduced cost," says Teo Yatman, vice president of business development.

Sigrity licenses OptimizePI for a $35,000 annual subscription. That price may seem high for a typical PCB tool, but Fang says it is in line with analysis-class PCB tools and is reasonable if you take into account the amount of savings your design project will gain from avoiding the overuse of decoupling capacitance. Fang claims that some beta users of the tool cut capacitance by 50%, drastically reducing the overall cost of their product and saving board space. "If you save even 20 cents for a volume product, that is, say, 20 million units, you'd save $4 million," says Fang.

Fang also claims that, because the tool is highly automated, you need no power-integrity-engineering expert to run it. He notes that designers can use the tool during several steps in PCB and package development. For example, they can use it during design to figure out the lowest cost configuration and to get a better idea of open board real estate during layout to implement the best configuration after placing the other components in the design, and even during manufacturing if other more inexpensive units become available or if a previously targeted unit becomes unavailable.

—by Michael Santarini

▷**Sigrity Inc**, www.sigrity.com.



(a)

Sigrity's OptimizePI automatically picks the right amount and lowest cost decoupling-capacitor scheme for your layout (a). It helps teams use just the right amount of capacitance to make performance goals. The black areas show the decoupling-capacitor count before (b) and after (c) using the tool.

NEWS FROM ESC

BY ROBERT CRAVOTTA

ARM updates RealView tools

At this month's ESC (Embedded Systems Conference) in San Jose, CA, ARM announced Version 3.1 upgrades to its RealView Development Suite for the full line of ARM processors. The update provides performance improvements and better tuning for ARM processors, most notably for the Cortex family of processors and the new Cortex-M1 processor, which ARM recently announced jointly with Actel (www.actel.com). The processors reside on an FPGA. Actel has licensed the Cortex-M1 processor and has made it available at no additional charge for designers to use the core in Actel's flash-based M1-enabled Actel Fusion programmable system chips and ProASIC3 FPGAs. The RealView Development Suite 3.1 is the first tool suite to support the new Cortex-M1 processor, and it includes an instruction-set-system model. Version 3.1 maintains interoperability with the RealView Create family of ESL (electronic-system-level) design tools and models. ARM now integrates the RealView Development Suite into the open-source Eclipse integrated development environment.

The tool suite features a new optional microlib C library, a subset of the ISO (International Organization for Standardization)-standard C runtime library, which ARM minimized for microcontroller applications. It achieves a 92% reduction in runtime-library-code size. Designers using ARM's Neon SIMD (single-instruction-multiple-data) signal-processing architecture can also separately license an add-on vectorizing compiler that complements the RealView Development Suite 3.1. The RealView ICE Version 3.1 run-control unit and its RealView Trace module, along with RealView Development Suite 3.1, now offer extended support for the ARM CoreSight debugging and trace technology, including multiple trace streams through a single port. The upgrade also supports the CoreSight single-wire-debugging interface. New intrinsics support for ARM DSP instruction-set extensions, ETSI (European Telecommunications Standards Institute) functions, and Texas Instruments (www.ti.com) C55x DSPs allows designers to write their signal-processing code with C intrinsics rather than assembly language. Version 3.1 supports the latest ANSI C99 language standard. Leading ARM partners are now using the suite, and it will become generally available in the second quarter of 2007.

▷**ARM**, www.arm.com.

Hi-Tech Software introduces call- and pointer-graph-based compilation

At ESC, Hi-Tech Software, a supplier of compilers for Microchip (www.microchip.com) and Cypress (www.cypress.com) microcontrollers, announced the OCG (Omniscient Code Generation) compilation technology that generates object code based on call and pointer reference graphs. The technology derives these graphs from examining all the modules in an embedded program before the final step of code generation. This global-optimization approach allows the compiler to catch inconsistent calling conventions, variable declarations, and redundant code because it examines all of the code before generating the final code. This approach allows the compiler to optimize the size of each pointer variable, based on its usage, resulting in smaller code. This process requires no extra input from the programmer and no nonstandard extensions, and it is entirely transparent. It identifies recursively or re-entrantly called functions and uses dynamic-stack space or local variable storage to ensure that re-entrant calls do not overwrite existing data.

The C language assumes a single linear address space. However, many embedded processors have complex, nonlinear memory architectures with different word widths. This fact makes it difficult to map non-target-specific C code onto some processors' memory maps. OCG creates a global representation about the complete set of variables and pointers across all program modules; it also knows how big the stack must be and where it will reside before generating the code. This approach allows the compiler to define a set of address spaces for each pointer variable that is optimally efficient for the processor architecture without any direction from the programmer. OCG builds separate call graphs for both mainline and interrupt code. Any function that appears in more than one call graph can replicate its own local variable area, eliminating the requirement for a separate stack. The current OCG implementation assumes that the entire project's call and pointer graphs can reside in the host computer's memory at once. This limitation does not exist in the current processor because the applications are smaller than the host computer's available memory.

PICC-18-Pro, the first compiler to implement OCG, achieves as much 13.4% better code density than Hi-Tech's previous-generation PIC18 STD compiler. PICC-18 Pro integrates into Microchip's MPlab integrated development environment as well as most third-party development tools. PICC-18 Pro runs on multiple platforms, including Windows 2000, Windows XP, Linux, and Macintosh OSX. Hi-Tech Software also offers the Hi-Tide 3 Eclipse-based IDE, including full project management; a flexible editor; and a fast, accurate simulator. PICC-18 Pro is available with full source code to all library routines and runtime-start-off modules, allowing programmers to customize the runtime environment for their hardware systems. There are no restrictions or limitations on the use of executable library code. You can download a free, fully functional, 45-day trial version of PICC-18 Pro from Hi-Tech's Web site. For a limited time, the $1195 PICC-18 Pro, is available for $895.

▷**Hi-Tech Software**, www.htsoft.com.

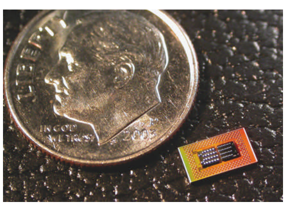
RESEARCH UPDATE

BY MATTHEW MILLER

Big advances come to tiny optical components

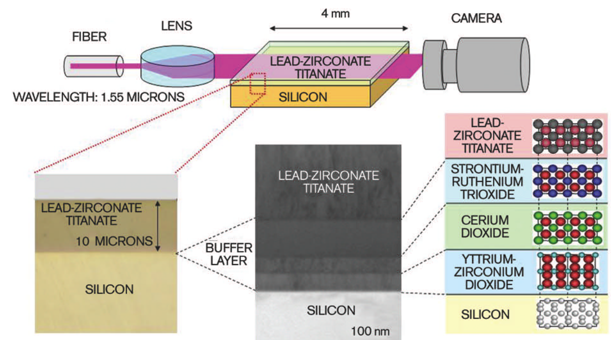
Last month's 2007 Optical Fiber Conference shed light on the industry's ongoing war against bulky, costly components. Two of the most notable advances involved efforts to move the production of optical components into the realm of cheap, proven silicon-process technology.

The Tokyo Institute of Technology (www.titech.ac.jp) and Fujitsu Laboratories (jp.fujitsu.com/labs/en) announced that they have successfully propagated infrared light through an optical-crystal film on a silicon substrate. This achievement, according to the researchers, paves the way for chip-level integration of silicon circuitry with optical devices, such as modulators and switches.



A 16-channel, full-duplex optical transceiver, built using standard process technologies, achieves data throughput of 160 Gbps (courtesy IBM).

In the past, when the researchers laid crystal films atop silicon, the films tended to exhibit jumbled atomic alignment that inhibited light propagation. The researchers solved this problem by placing a single-crystal film of PZT (lead-zirconate titanate)—a material known for its excellent optical properties—atop a three-layer buffer of other materials. The use of the buffer resulted in minimal disruption of the PZT layer's atomic alignment, which translated to one-tenth as much signal loss as other technologies for the 1.55-micron wavelength of light in optical-communication applications, according to the researchers.



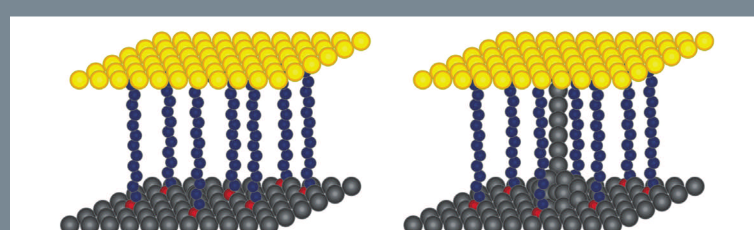
A sandwich of materials enables effective propagation of 1.55-micron light through a PZT (lead-zirconate-titanate) crystal film atop a silicon substrate (courtesy Fujitsu).

Also at the conference, IBM (www.ibm.com) researchers unveiled a prototype optical-transceiver chip that boasts throughput of 160 Gbps—eight times faster than today's standard-issue optical components. The 3.25×3.25-mm package combines a CMOS optical transceiver, including driver and receiver circuitry, with optical components constructed from materials including indium phosphide and gallium arsenide.

▷**Optical Fiber Conference**, www.ofcnfoec.org.

NANOELECTRONIC SWITCH HARNESSES SILVER WHISKERS

Researchers at NIST (National Institute of Standards and Technology) have demonstrated a prototype nanoscale electronic switch that exploits a troublesome characteristic of silver as "a feature, not a bug." With its high conductivity, silver would make an excellent material for circuitry were it not for the tendency of silver ions to form tiny, short-circuit-causing "whiskers" when exposed to electric fields.



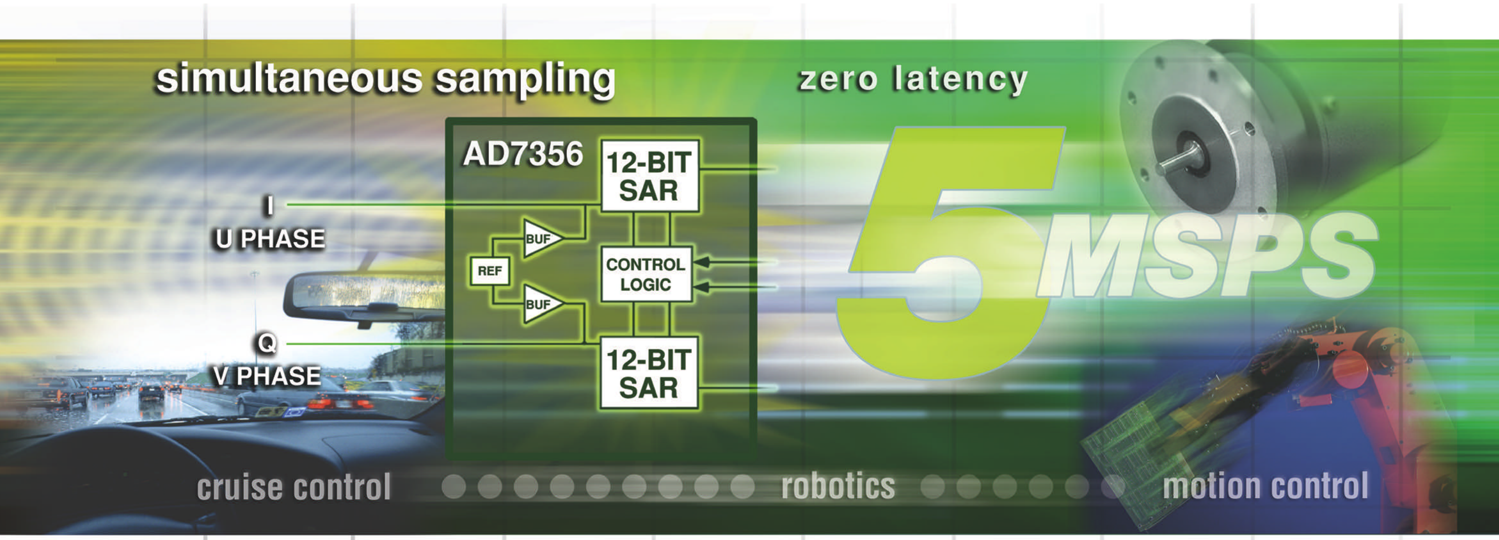
A silver-ion whisker grows to bridge the gap between silver and gold wires in a prototype nanoelectronic switch when off (left) and on (right).

The NIST device capitalizes on this whisker growth, employing it as the mechanism that closes a connection between a silver wire and a gold wire laid perpendicularly on top of it. The application of a small voltage induces the silver wire to sprout a filament that grows quickly through an organic-molecule coating until it reaches the gold wire, causing a large change in conductance. Reversing the voltage retracts the whisker, reopening the switch.

The researchers claim that the technology is attractive for nanoscale-memory devices because it works with a variety of self-assembling organic materials, the simple grid structure lends itself to large arrays, and the resistance ratio between the off and the on states is more than 1 million-to-one. Drawbacks researchers have yet to overcome include a switching speed of only 10 kHz in the prototype and a tendency of the switches to freeze closed after "a large number" of cycles.

▶**National Institute of Standards and Technology, www.nist.gov.**

5 million reasons why SAR ADCs mean ADI. In motion control, analog is everywhere.



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ANALOG DEVICES

BY HOWARD JOHNSON, PhD

Diagnostic testing (and tasting?)

In 1971, I enjoyed one blissful summer away from school working in a TV-repair shop. The first day on the job, my boss, Paul, explained how to work with customers at the repair counter: “Mainly, use your sense of smell. If it’s just dusty, that’s probably fine. If it smells like a burned resistor or burned capacitor oil, that’s going to cost. If it smells like baked milk, tell me, and I’ll sell ’em a new set. They already know their kid spilled milk into it, so they feel guilty. I’ll have the new set in place before hubby comes home.”

Wow! I had a lot to learn, and fast. Paul used all of his senses diagnosing a broken set. He could feel the 60-Hz hum from the power transformer, see the blue ionizing glow of a bad tube, hear the squeal of the 15-kHz horizontal oscillator, and smell the difference between a blown capacitor and a burned resistor. As for taste, Paul licked the terminals of a 9V battery to tell whether it was any good.

Today, human senses play a smaller role in diagnosing digital systems, but the philosophy remains the same: Use every tool at your disposal. Stick your hand into the chassis to feel the airflow. Touch the processor to see how hot it’s getting. Listen to the disk chatter. Gather as much information as possible.

Compliance testing rests at the opposite end of the test spectrum. A compliance test begins with a specific list of features or performance metrics that you must verify. The test determines whether a system meets the acceptable criteria. If the system fails, the operator either discards the unit or sets it aside for rework. He makes no attempt at diagnosis.

The most interesting part of compliance testing happens before you hook up the first device under test. You must prove that your test-equipment configuration works, and works well enough to make the required measurements.

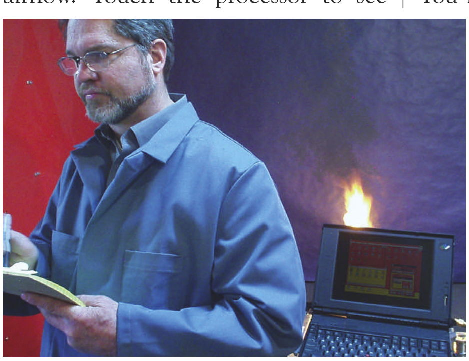

Figure 1 A test professional pays close attention to every aspect of testing.

The diagnostic process, in contrast, is a more broadly based activity. It requires a keen awareness of all aspects of the system at hand. The operator must remain ever-vigilant during testing, aware of even the tiniest clue about system behavior (**Figure 1**).

David Agans, in his terrific book, *Debugging*, articulates a coherent nine-point strategy for debugging that involves, first, deciding when to invoke the strategy (**Reference 1**).

As an everyday matter, you aren’t going to walk around trailing a cart full of data scopes, recording analyzers, and EMI detectors, because that would be too much of a hassle. You need not record everything, or take careful notes, or think before you act, as long as everything goes smoothly in the lab. You instinctively know how to tweak your schematic to casually fix the obvious problems that crop up.

To help keep things easy, break the system down into small pieces—so small that there is likely only one error (or no errors) in each section. Taken in small sections, problems tend to stand out in an obvious way. That makes debugging a snap.

The time to apply your high-level-debugging expertise is when things start to look ugly. Systems that harbor multiple errors often display inexplicable, impossible, or unreliable behavior. When that situation occurs, start thinking like Paul.

Take careful notes, augment your senses with recording devices that capture the history and current state of your equipment, and spend as much time thinking and planning for the next test as you do in the lab gathering data.EDN

REFERENCE

1 Agans, David, *Debugging*, Amacom, September 2006, ISBN 978-0814474570.

MORE AT EDN.COM

Check out Howard Johnson’s videos at www.edn.com/techclips.

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

BY CLARK ROBBINS • GS ENGINEERING

Answers can be anywhere

DANIEL VASCONCELLOS

When I was a young engineer, my boss asked me to design a discrete-logic controller for a mechanical/hydraulic apparatus. After weeks of work using CMOS logic and power transistors, I reanalyzed the design, and everything seemed correct. I then commissioned prototype PCBs (printed-circuit boards), and, by the time they were ready, I had enough parts to build some samples. I used switches and lights to simulate the apparatus. Again, everything worked OK. When I connected my controller to the first apparatus, everything still worked fine. Even after the engineers had tested everything using my controller, there were no major problems.

The team involved with the mechanical/hydraulic-apparatus design discussed how it would handle production. Because my work with the controller was essentially done, I volunteered to design an automated-test system. Although I tried to hide the anticipation of designing my first microcontroller system, I was elated when my boss gave me the task and got management to sufficiently fund it.

This part of the project turned out to be significantly more complicated than the original controller design, involving hardware design and software programming in assembly language. The test system would have to be able to power the complete apparatus. It would also have to cycle through all the modes, monitor the hydraulic solenoids and wiring to make sure that there were no shorts or opens, and simulate and control the same outputs as the apparatus controller would. Finally, it would need to accomplish all of these tasks under the control of a software program running the microcontroller chip.

This system was new and had bugs and idiosyncrasies. And though I eventually got it running, I was now behind schedule. After completing the automated-test-system-hardware design, I was working hard at learning the language for this new microcontroller. I don't remember my professor's saying that not all microcontrollers have the same assembly language. I figured that they would all be similar to the one I had learned about in class. Big mistake. The instructions were significantly different from what I had learned. I was beginning to worry that I wouldn't make the schedule.

The programming and debugging were not going well. In addition, I was having hardware problems. I was now working 12 hours a day, but, just when things were starting to improve, the black clouds came overhead.

Reconnaissance suggested to me that my system problem could be an error in the software program. I found and fixed some bugs, but the problem was still there. So, I spent hours debugging the system. Things were again looking bad for the schedule, despite the fact that I was now working 14 hours a day. For three or four days, I worked on nothing else yet made zero progress. I was so focused on one area that I was not looking anywhere else.

Then, I got really lucky; a student working for me suggested that I look at one of the PCBs. Though I disagreed with his suggestion, I decided to pursue it. (I did not want to discourage him from sharing future ideas.)

After probing some of the circuits, I found a problem with a Schmitt-trigger IC. Once I replaced the IC, the automated-test system worked the way it was supposed to.

Throughout my career, I have achieved some measure of success by developing a reputation for being able to solve problems. The lessons I learned during this project became ingrained in me and became the cornerstones of this success. I try never to dismiss a suggestion from anyone, regardless of the person's job, background, or education. And I try never to focus so narrowly that I miss the big picture, where a problem's source might reside. **EDN**

__Consultant Clark Robbins is a software-application engineer. You can share your Tales from the Cube and receive $200. Contact Maury Wright at mgwright@edn.com.__

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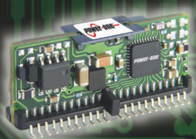
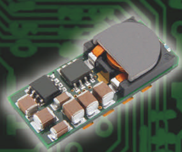


Z-Series Digital POLs



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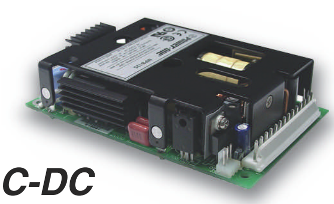

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LSI'S ZEVIO PROJECT SHOWS THAT SUCCESS IN CONSUMER ELECTRONICS DOES NOT ALWAYS MEAN IMPLEMENTING THE FASTEST SOC IN THE LATEST AND GREATEST PROCESS TECHNOLOGY.

SQUEEZING A LOW-COST MULTIPROCESSOR PLATFORM OUT OF 130 NM

Figure 1 LSI Logic's Zevio 1020 was the main processing unit for the VTech V.Station.

BY MICHAEL SANTARINI • SENIOR EDITOR

Sometimes designing an SOC (system on chip) on the latest and greatest process technology is not what it takes to make an impact on the cost-conscious consumer-electronics market. That's a lesson LSI Logic engineers took to heart in designing LSI's Zevio 1020 multimedia-application-processor platform.

In December 1994, educational-electronics company VTech and IP (intellectual-property) developer Koto commissioned the company to create a multiprocessor SOC to run VTech's VFlash "edutainment system" (**Figure 1**). Traditionally an ASIC vendor, LSI Logic has over the last few years been transitioning to selling standard products. So, when VTech commisioned LSI to create an SOC, LSI's management decided to turn what would have traditionally been an ASIC design into a general multimedia-processor platform.

Shinya Fujimoto, architect of the Zevio project, says that his design group at LSI had to work within several constraints: Create a multiprocessor platform that was generally modular, so LSI engineers could swap out blocks to quickly create derivative products; implement the SOC on a mature, 130-nm, low-power process technology to keep costs reasonably low and still hit performance and power goals; and, finally, finish the initial SOC platform in nine months.

"Our background was consumer ASICs," says Fujimoto. "Our group did chips in the PlayStation and PlayStation 2 and some of the iPod designs, and, during the development of those [products], we noticed that we were spending a lot of time redefining the noncritical part of the chip…That's why we decided to develop this architecture."

Fujimoto says that the first step in defining the Zevio architecture involved meeting with the VTech and Koto system architects. "We try to get as much feedback and even complaints from the customer to define where the potential bottlenecks are going to be in the design process," he says.

The Zevio, Fujimoto claims, is not a typical application processor (**Figure**

2). "It's what I call a heterogeneous multiprocessor," he says. "It has multiple processors that are not the same but run in parallel, and each of the processors [is] dedicated to certain tasks they are good at."

The group determined that the SOC would incorporate an ARM9 processor for generic processing. The LSI team would create a custom graphics processor and audio- and memory-controller cores, and the design would incorporate an LSI Logic ZSP DSP core to do more immediate decoding and codec-type applications. "The key for us was to have multiple processors that run independently"—meaning, according to Fujimoto, that each becomes its own master and completes its operations without CPU intervention. "We had to make sure that they could all run efficiently without causing a bottleneck on the bus or the memory."

Implementing the design on a mature, low-power, 130-nm process (from an undisclosed partner in Taiwan) instead of a 90- or 65-nm process helped keep chip costs down, stabilize power management, and avoid the use of DFM (design-for-manufacturing) tools, all to speed the design process. The chip targeted applications for systems that cost less than $100, says Fujimoto. "Anyone can make a huge chip, but some people, especially video-game vendors who will remain nameless, are struggling now because of increased chip costs going into consumer products."

AT A GLANCE

- LSI implemented the 2 million-gate Zevio 1020 in 130 nm instead of 90 nm.
- LSI designed a new 16-bit graphics processor and memory controller and modified the AHB.
- The actual design took nine months, excluding spec work.
- LSI derivatives will take only six months to produce.

Fujimoto notes that many companies are too quick to jump to the latest and greatest new process when they could have accomplished more with a more mature and stable process, such as 130 nm. "Some people left the 130-nm segment just because it is considered lower end, but we felt we could create a high-end design through smart engineering. Customers hear stories from competitors about high-performance this and that—all the flashy terms—but in the end, it comes down to [getting] the best bang for your buck." He maintains that the maturity of the 130-nm process, its cost, and its performance made the best fit.

LSI wanted Zevio to be a reusable platform, not just an ASIC, so a key component was creating unique cores that you could combine with a range of LSI or even third-party vendor cores. However, a major component of the architecture specification was a new graphics-processor-core design. LSI worked with IP-vendor Koto to develop Zevio's 3-D-graphics-processing core. Fujimoto notes that several of the Koto engineers previously worked on the Nintendo GameBoy design team. LSI had little experience in this area and so welcomed Koto's experience, says Fujimoto. "[The engineers] provided a lot of insight into the features software developers need and helped us transfer a lot of that know-how into hardware."

Koto's team did most of the specification work and verification on the core, and LSI designers handled the design and RTL implementation of the core. The 16-bit, 3-D-graphics core requires only 300,000 gates and consumes 20 mW running at 75 MHz, which allows it to draw 1.5 million polygons per second.

Fujimoto pointed out that another potential bottleneck was the memory controller and its interface to the system memory. Although, as chip designers, it would have been easier for them to work

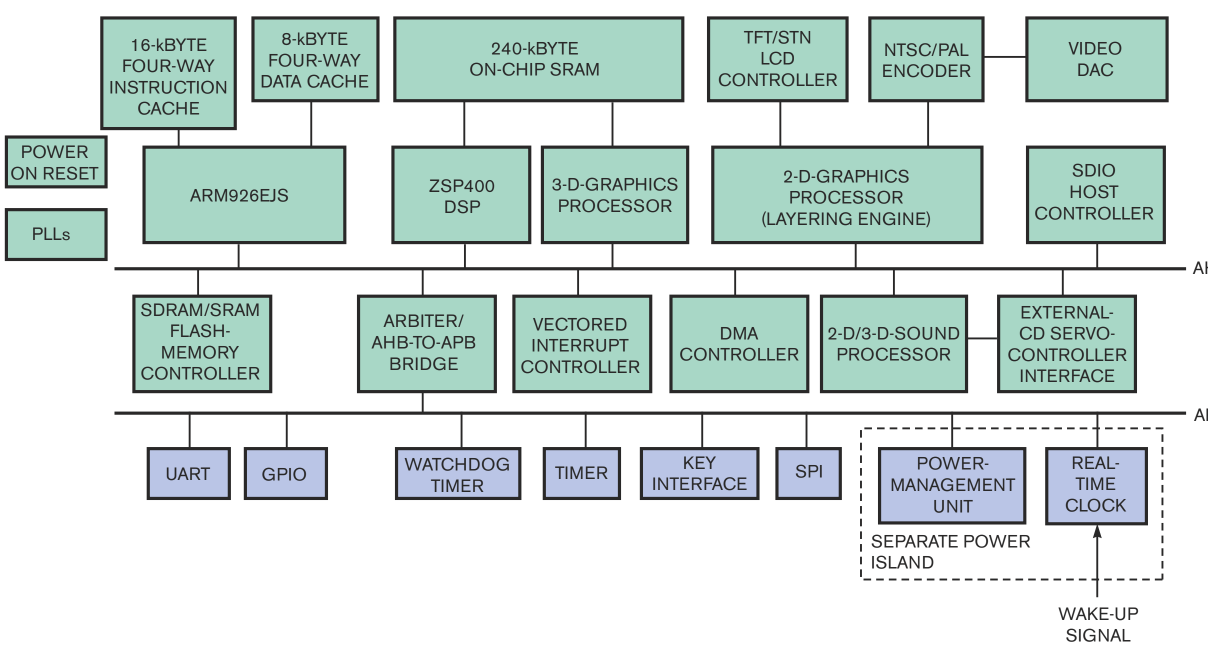

Figure 2 Zevio's platform architecture incorporates several dedicated processor cores running on a modified version of ARM's AMBA AHB.

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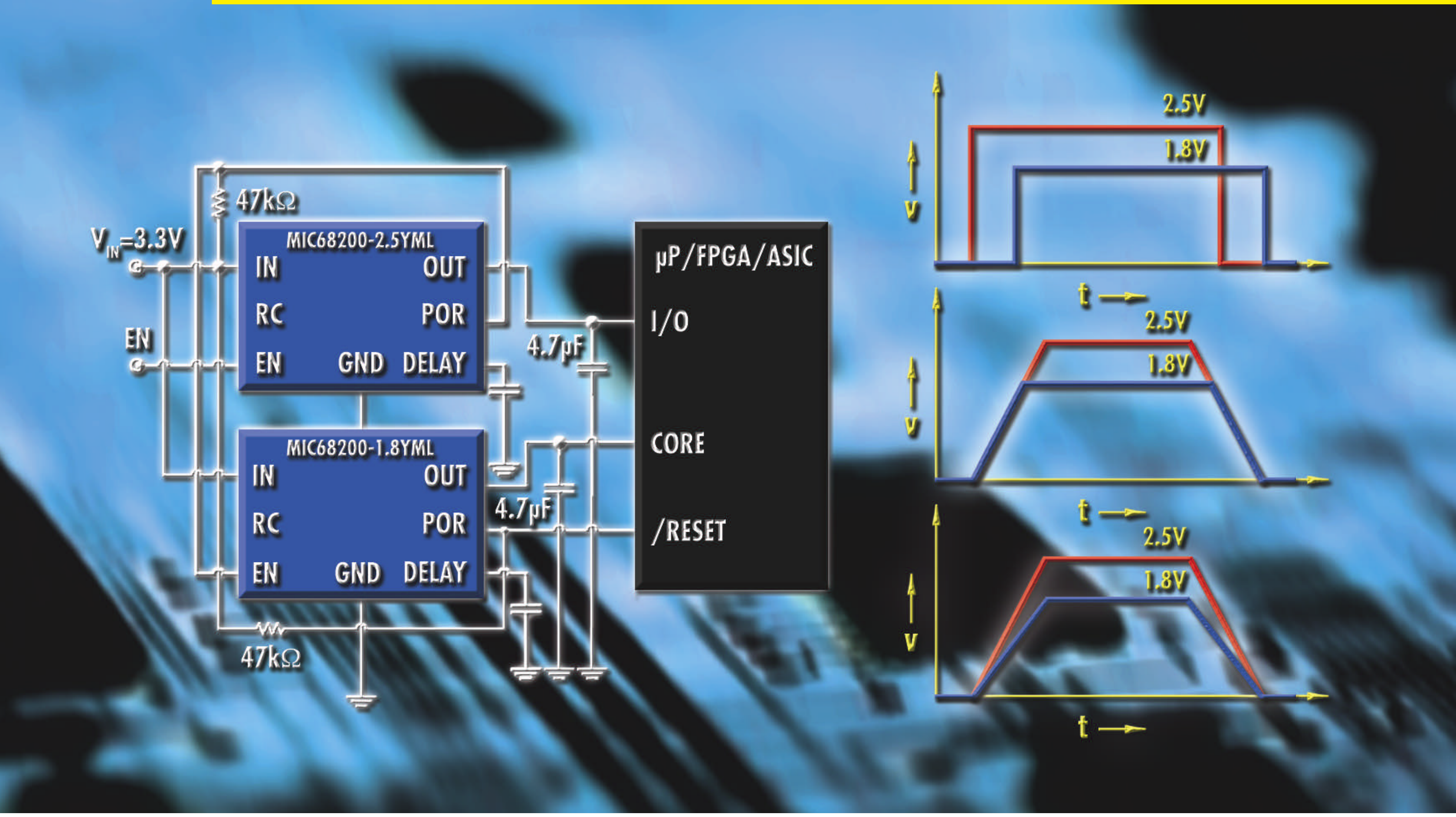

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with a 32-bit bus interface, run it fast, and obtain the desired performance, LSI had to figure out how to get the same performance from a 16-bit interface memory, to reap the cost benefits.

The team had to design from scratch an efficient controller core that would use a 16-bit interface and allow for efficient arbitration. "What we figured out when we looked at a 16-bit interface was that we could get a nice timing window where we [could] issue many commands to the SDRAM," says Fujimoto, who notes that the controller can fetch two words for every bus-clock cycle. "We're patenting that technology. It allows us to efficiently use these timing slots to open up multiple banks." Fujimoto views this development as the key innovation in the architecture.

The team wrote RTL for the controller and then ran proof-of-concept simulations. "We saw a lot of improvement over typical designs of memory controllers," he says. "At that stage, we proved that we could get good performance on a 16-bit interface."

Fujimoto says that next the group had to look at the related bus-protocol bottleneck. The group decided to use the popular ARM AMBA (Advanced Microcontroller Bus Architecture) AHD (AMBA high-speed-bus) protocol but had to figure out ways to overcome some of AHB's inefficiencies. "We had to look at its inability to do burst writes to random addresses and its inability to specify large enough burst writes," he says. To work around these issues, the group wrote its own extensions to AHB, which helped double the memory controller efficiency.

After working out the larger issues of the specification phase, the design group, which ranged at times from 10 to 15 design and verification engineers, began work on the RTL design. Fujimoto broke his team into subteams. "One team focused on the memory controller, one on the graphics core, another on the audio core, and another team on the overall integration," he says.

Fujimoto says that LSI's traditional methodology is to have each subteam design and then verify the individual blocks and then verify the blocks with other cores in the system using simulators. But for the first time, his team this time employed an FPGA-prototyping system to run verification and hardware/software validation on the graphics core, memory controller, and an audio processor LSI developed.

"There would have been too many corner cases to validate this design just in a simulation environment," says Fujimoto. "This [instance marked] the first time our group used an FPGA-prototyping system. In retrospect, we should

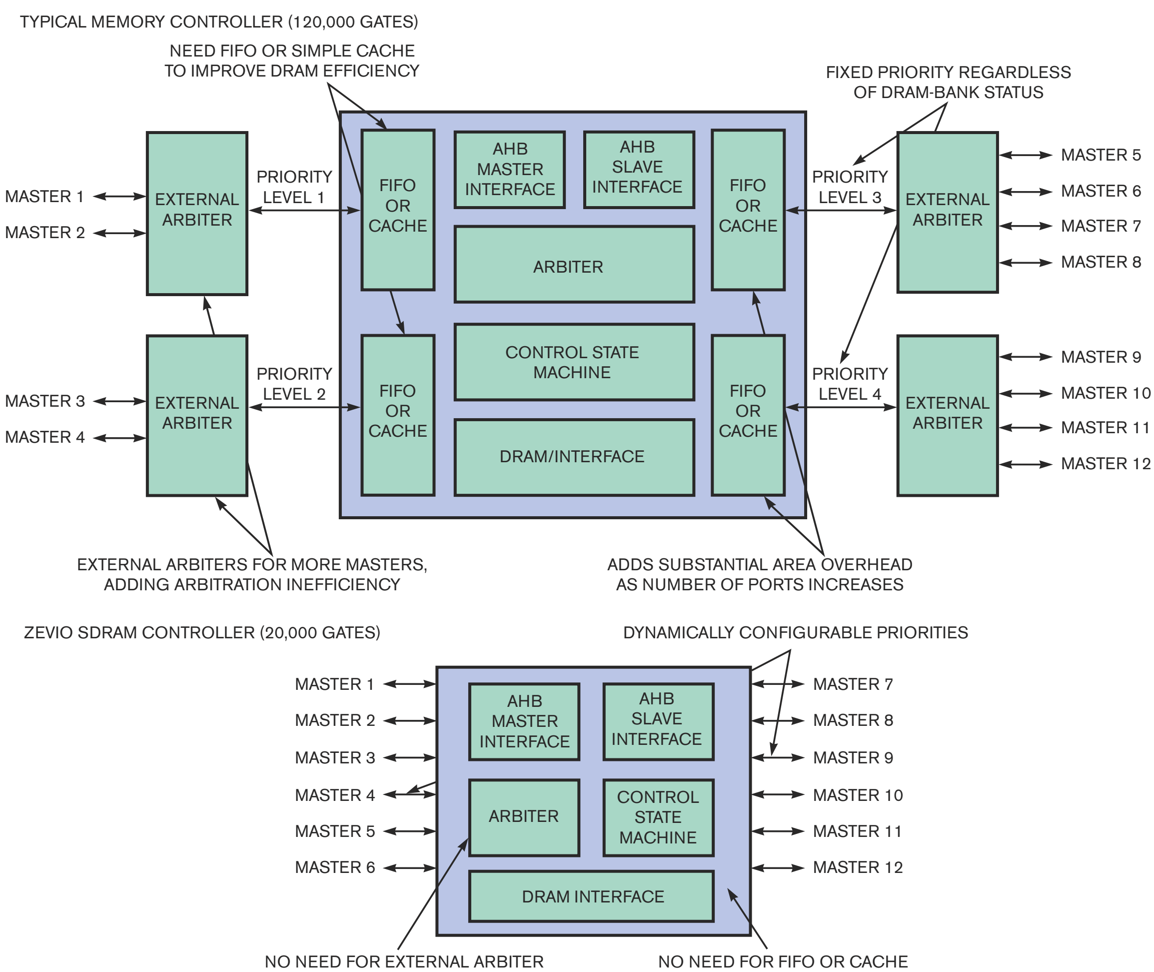

Figure 3 LSI designed a new 16-bit memory controller core that fetches two words for every AMBA AHB clock cycle.

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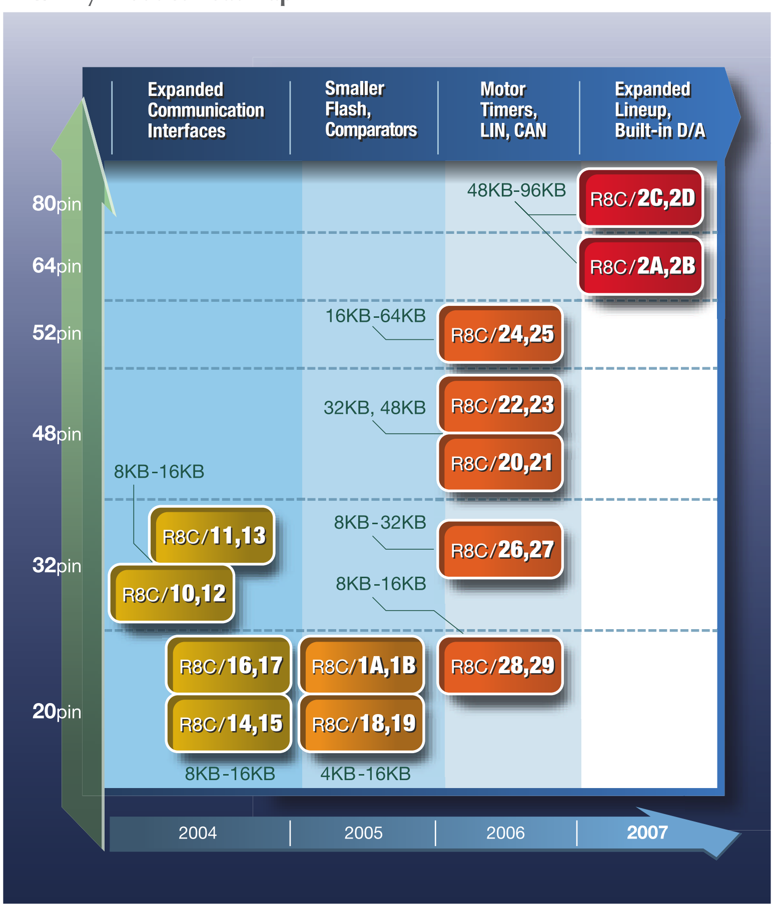
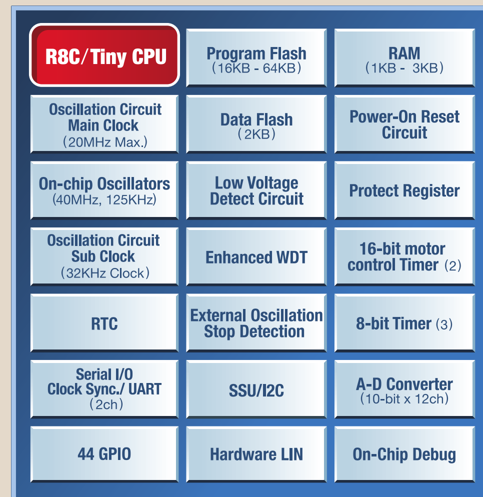


HOT Products R8C/25



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*Source: Gartner Dataquest (April 2006) "2005 Worldwide Microcontroller Vendor Revenue" GJ06333 have done a bit more verification on the individual cores earlier in the design." Fujimoto recalls that, once the FPGA system was working, things progressed quickly: "When we ran into problems, we could see them on the LCD screen hooked up to the FPGA-prototyping board. We could simply stop the debugger and look at the internal registers where the error occurred."

The team also ended up chasing down bugs that turned out to be glitches in the FPGA-programming software, not the design. "We didn't realize we were tackling bugs that were caused by the tool vendor," says Fujimoto. "We used the FIFO controller provided by the FPGA vendor, [which] also had a problem."

Fujimoto notes that the graphics team created a C model of the graphics core during the spec phase. "We would have used the C model for the verification, but it was too much work to update the C model as well as the RTL," says Fujimoto. That C-model methodology works if you have a fixed specification, he notes, when you can use the C-model output to verify RTL output.

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In LSI's case, however, the spec wasn't 100% complete when the team started RTL: "We dropped the C model once our FPGA system was up and running," he says. The group also started preliminary driver development once it stabilized the design on the FPGA-based prototyping system.

The prototyping board served as the basis for a validation board that LSI now offers customers wishing to develop other systems with Zevio SOCs. After the group had stabilized the RTL, the team ran a trial synthesis and a trial layout, filling in portions of the preliminary layout with "blank gates" to get a rough idea of the area and die size. Fujimoto says that his group uses Synopsys for synthesis and Magma for place and route.

Fujimoto says that the trial layout was especially important for determining the correct placement of the memory blocks. The design incorporated 240 kbytes of SDRAM. Therefore, the Zevio layout team had to work with the RTL team to break up the blocks to ensure that the various cores could efficiently access the memory and not take up too much room in the layout. "We had this big memory, but we allowed both the graphics engine and the DSP to access the same memory," he says. "At the functional register, we assigned which core gets access to the memory and what it will access, so we had to predefine certain segments for the DSP and graphics engine." To achieve this goal, the layout and RTL group went through several iterations to determine the optimum layout of the memory. In the end, the entire Zevio SOC consisted of 2 million gates.

To help keep the design low power, the group used a multivoltage-threshold, 130-nm library. "The idea was to synthesize the entire design with all low-leakage, low-performance gates and then identify the bottlenecks in the timing and the critical path and convert those paths into high-speed gates," says Fujimoto. Following that process al-

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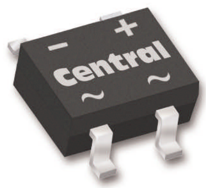

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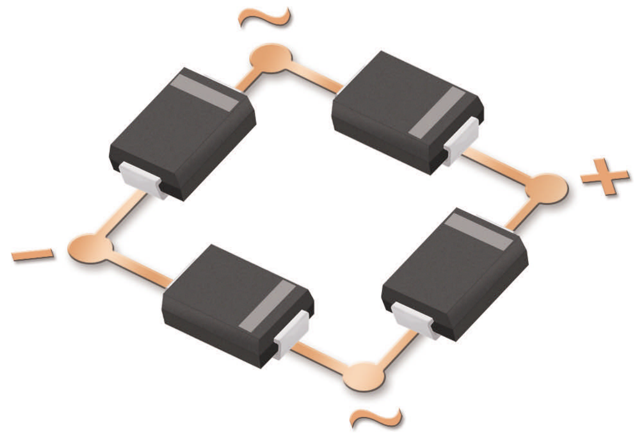

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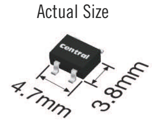

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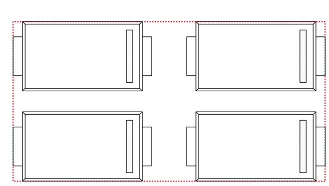

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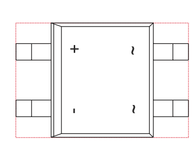

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lowed the team to achieve the right mix of low-leakage and high-performance transistors.

Physical verification and tapeout of the design went fairly smoothly, says Fujimoto. "The prototypes [silicon] came, and, three days later, all our demos were running on the real system," says Fujimoto. "[The customers] were able to go home a week early … Going with a mature technology along with the validation and prep work we did early in the process really paid off."

The fast board "breakup" also meant that software teams at VTech could quickly move into product development and ultimately allowed VTech to introduce its system to the market in time for Christmas 2006.

But VFlash isn't the only application of the Zevio product line. In fact, Fujimoto says that, because the design group made the SOC modular, LSI teams can tailor it for other customer applications. "We designed the platform with the goal [of creating] derivatives of the platform in only six months," says Fujimoto.

He notes that the modular platform allows users to fairly easily swap out the ARM core for a MIPS core because LSI has licenses for both. Users can also swap out several of the peripheral cores. LSI is working on adding USB support to the system. Fujimoto says that next-generation Zevio platforms will also likely incorporate DDR instead of SDRAM. Although Koto created the original operating system for the platform, LSI is expanding the number of operating systems the platform supports and is now working on Linux OS and Windows CE.

Fujimoto says that his group has finished another project on Zevio for an unnamed customer. He says that the silicon is in production but the customer has not yet introduced the product.

LSI began the Zevio specification process in December 2004, started the design at the end of 2005, and went into production nine months later in September 2006.

The Zevio project is yet another example that success in the consumer market is not always equal to implementing the fastest SOC in the latest and greatest process technology. With a lot of planning at the architecture stage and a bit of creative engineering along the way, the LSI team created a relatively powerful, cost-effective platform that helped VTech hit its market window and gave LSI a versatile tool to help other customers do the same. It will be interesting to see how long the Zevio remains a viable platform for LSI and how many derivatives the company can spin for other customers. EDN

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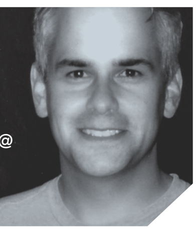

BY PAUL RAKO • TECHNICAL EDITOR

MEASURING nanoamperes

MEASURING LOW CURRENTS CAN BE TRICKY. CLEVER ANALOG-DESIGN TECHNIQUES AND THE RIGHT PARTS AND EQUIPMENT CAN HELP.

Thousands of applications require a circuit to measure a small current. One of the most common is the measurement of photodiode current to infer the light impinging on the diode. Scientific applications, such as CT (computer-tomography) scanners, gas chromatographs, and photo-multiplier and particle and beam monitoring, all require low-level current measurements. In addition to these direct applications, the manufacturers of semiconductors, sensors, and even wires must measure extraordinarily low currents to characterize their devices. Leakage current, insulation-resistance measurements, and other parameters require consistent, accurate measurements to establish data-sheet specifications.

Few engineers realize, however, that the data sheet of a part is a contractual document. It specifies the behavior of the device, and any disputes over the operation of the part always come down to the specs on the data sheet. Recently, a customer of a large analog-IC company threatened legal action against the manufacturer, claiming that the parts he had purchased exhibited far higher operating currents than the submicroampere levels that the company specified. It turned out that the PCB (printed-circuit-board)-assembly house was properly washing the board but that assemblers were picking up the PCB and leaving fingerprints on a critical node. Because it could measure these tiny currents, the semiconductor company proved that its parts were working correctly; the leakage current was due to dirty PCBs.

The difficulty with measuring small currents is that all kinds of other effects interfere with the measurement (see **sidebar** "History of current measurements" at www.edn.com/070426cs). This article looks at two breadboard circuits that must handle surface leakage, amplifier-bias-current-induced errors, and even cosmic rays. As in almost all circuits, EMI (electromagnetic interference) or RFI (radio-frequency interference) can induce errors, but, at these low levels, even electrostatic coupling can cause a problem. As the currents you measure drop into the femtoampere range, the circuits are subject to even more interfering effects. Humidity changes the value of capacitors and causes higher surface leakage. Vibrations induce piezoelectric effects in the circuit. Minor temperature variations, even from a room fan, cause temperature gradients in the PCB that give false readings. Even room light can degrade the accuracy of measurements; light from fluorescent fixtures can enter the glass ends of a detector diode and cause interference (**Reference 1**).


120
100

Small currents require accurate measurement if you want to characterize the performance of quartz-crystal oscillators. Jim Williams, a staff scientist at Linear Technology and longtime *EDN* contributor, shares a circuit he designed for a customer who needed to measure the rms current in a 32-kHz watch crystal (**Figure 1**). One difficulty with this measurement is that even a FET probe's 1-pF loading can affect the crystal oscillation. Indeed, one of the goals of current measurement is to establish the sizing of the low-value capacitor you use with every crystal oscillator. A further difficulty of this measurement is that it must measure accurately and in real time at 32 kHz, which rules out the use of an integrating capacitor. The signal is a complex ac signal that the system designer must convert to an rms value for evaluation.

"Quartz-crystal rms operating current is critical to long-term stability, temperature coefficient, and reliability," says Williams. The necessity of minimizing introduced parasitics, especially capacitance, complicates accurate determination of rms-crystal current, especially in micropower-crystal types, he says. **Figure 2**'s high-gain low-noise amplifier, he explains, combines with a commercially available closed-core current probe to permit the measurement, and an rms-to-dc converter supplies the rms value. The dashed lines indicate a quartz-crystal test circuit that exemplifies a typical measurement situation. Williams uses the Tektronix CT-1 current probe to monitor crystal current and introduce minimal parasitic loading. A coaxial cable feeds the probe's 50Ω output to A_1; A_1 and A_2 take a closed-loop gain of 1120, and the excess gain over a nominal gain of 1000 corrects for the CT-1's 12% low-frequency gain error at 32.768 kHz.

Williams investigates the validity of this gain-error correction at one sinusoidal frequency—32.768 kHz—with a seven-sample group of Tektronix CT-1s. He reports that device outputs are collectively within 0.5% of 12% down for a 1-μA, 32.768-kHz sinusoidal input current. Although these results tend to support the measurement scheme, Williams contends that it is worth noting that Tektronix measured the results. "Tektronix does not guarantee performance below the specified −3 dB, 25-kHz low-frequency roll-off. A_3 and A_4 contribute a gain of 200, resulting in total amplifier gain of 224,000. This figure results in a 1V/μA scale factor at A_4 referred to the CT-1's output. A_4's LTC1563-2 32.7-kHz bandpass-filtered output feeds A_5 through an LTC1968-based rms-to-dc converter that provides the circuit's outputs," he says. The signal-processing path, Williams explains, constitutes an extremely narrowband amplifier tuned to the crystal's frequency. **Figure 3** depicts typical circuit waveforms. According to Williams, the crystal drive at C_1's output (upper trace), causes a 530-nA rms crystal current that the A_4's output (middle trace) and the rms-to-dc-converter input (lower trace) represent. "Peaking visible in the middle trace's unfiltered presentation derives from parasitic paths shunting the crystal," he says.

AT A GLANCE

- Physics and noise limit the measurement of small currents.
- Early mechanical meters could resolve femtoamperes.
- JFET and CMOS amplifiers are suitable for measurements.
- To measure femtoampere-level currents, integrate the current into a capacitor.
- Integrated parts can measure femtoamperes and provide 20-bit outputs.

Williams' circuit provides several lessons. Measuring nanoamperes is difficult even when using integrating techniques. This problem was far more difficult, because he had to complete the measurement in real time. Further complicating matters was the fact that this ac measurement required a bandwidth of 32 kHz to capture the bulk of energy in the oscillator current waveform. Williams addressed these problems by using a sensor. The Tektronix CT-1 sensor (**Reference 2**) can cost as much as $500, but, without a good sensor, Williams would not have been able able to recover the signal from all the noise. In addition to good sensitivity, the CT-1 has a 50Ω output impedance that allows for lower noise-signal paths than would a high-impedance output. Another important principle that this example demonstrates is that it is essential to limit the bandwidth of the signal path. By making a narrowband amplifier chain, Williams discarded all the noise contributions from frequencies that were not in his area of interest. Finally, Williams used good low-noise design principles in the circuit. Wiring critical nodes in air minimizes leakage paths, and the LT1028 is

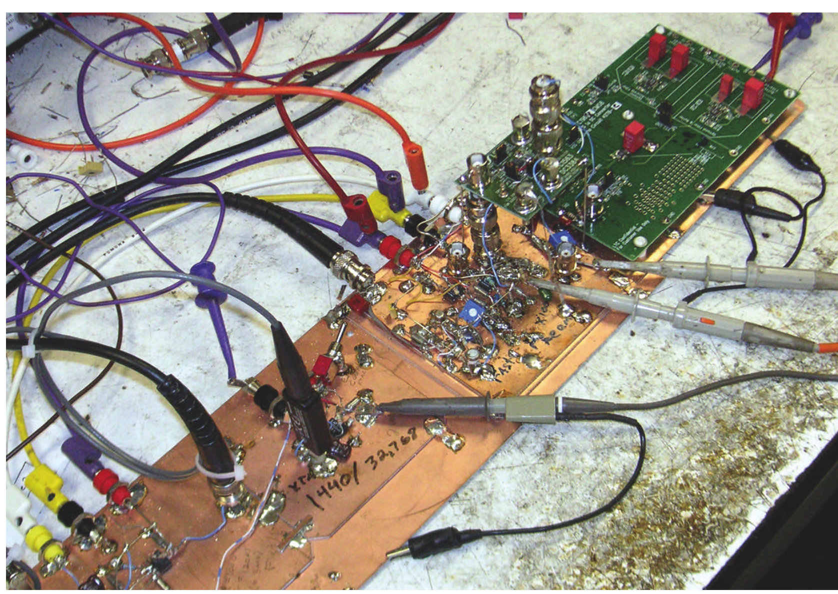

Figure 1 This breadboard measures the rms current in a watch crystal (courtesy Linear Technology).

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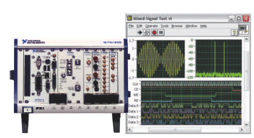

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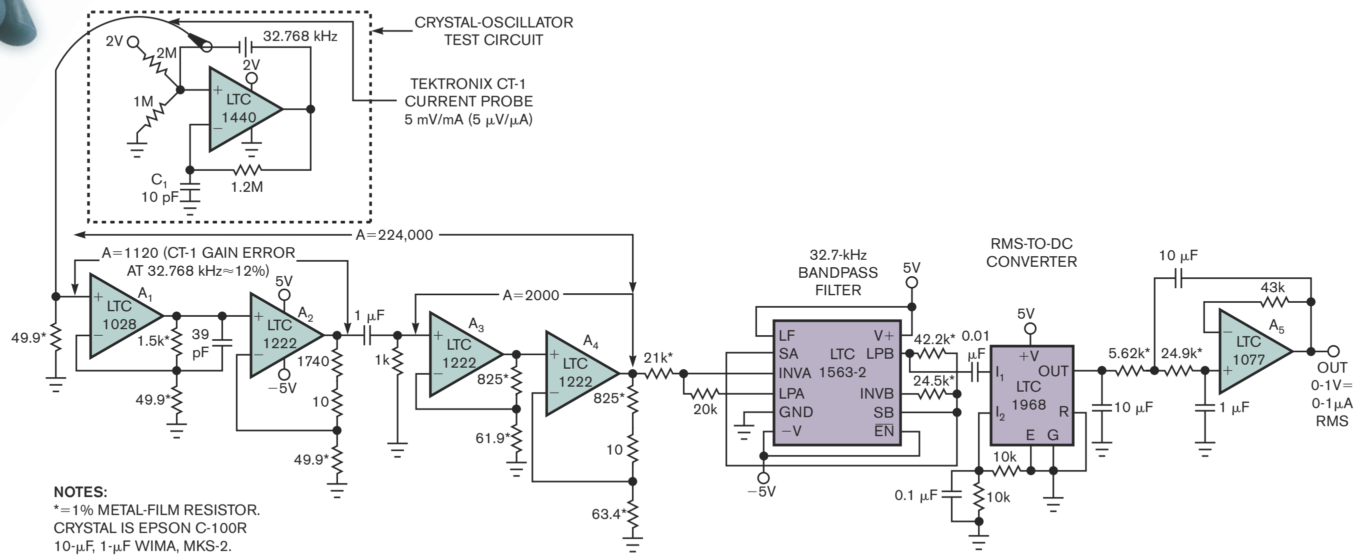

Figure 2 A_1 to A_4 furnish a gain of more than 200,000 to the current probe, permitting submicroampere current measurement. An LTC1563-2 bandpass filter smoothes residual noise and provides unity gain at 32.768 kHz. An LTC1968 supplies rms-calibrated output.

perhaps the lowest noise amplifier available from any manufacturer when working from 50Ω source impedance.

FEMTOAMPERE BIAS CURRENT

Paul Grohe, an application engineer at National Semiconductor, provides another remarkable example of measuring tiny currents. Years ago, National decided to sell the LMC6001, an amplifier that had a guaranteed bias current of 25 fA, implying that National needed to measure the bias current of each part to verify the specification. The test department could not accommodate test equipment in the setup; all the circuitry had to fit onto a standard probe card. Grohe and engineering colleague Bob Pease built a proof-of-concept fixture to demonstrate the feasibility of a small test circuit that could resolve to 1 fA (**Figure 4**). Many books and resources discuss using an integrating capacitor to measure small currents (**Reference 3**). The principle is that a small current can charge a small capacitor and that you can read that voltage to infer the current. In some cases, the current is an external current from a sensor. In this case, the current is leaving the amplifier-input pin. **Figure 5** shows a simple theoretical circuit in which the amplifier is measuring its own bias current.

The reality of measuring small currents is far more involved than the **figure** would suggest. First, Grohe could

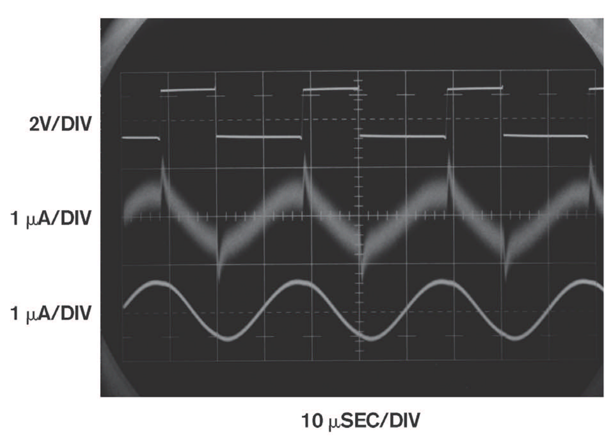

Figure 3 The upper trace shows C_1's 32.768-kHz output. A_4's output (middle trace) shows the crystal current. The lower trace shows the rms-converter input. Peaks in the middle trace's unfiltered presentation derive from parasitic paths shunting the crystal (courtesy Linear Technology).

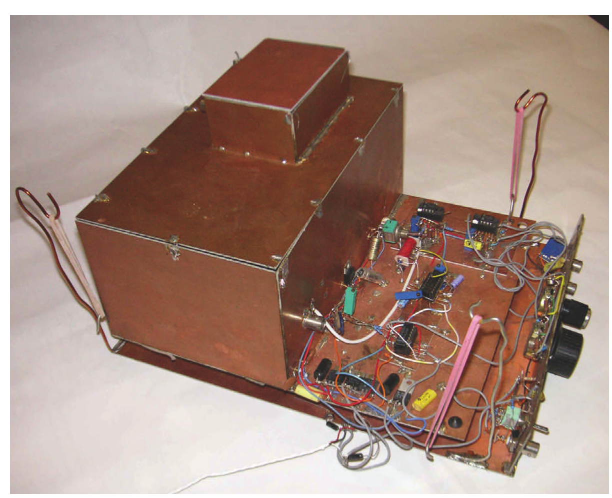

Figure 4 This prototype can resolve 1 fA of an amplifier's bias current. The breadboard has several levels of shielding made by soldering together copper-clad PCBs. Note the rubber-band suspension to shield the electronics from vibration (courtesy National Semiconductor).

not use the part itself to measure its own bias current. If he had tried to use the part itself as the integrator, there would have been no way to calibrate the effects of a socket and other leakages associated with the test fixture. Doing so required a separate low-bias-current part as the integrator (**Figure 6**). Using a CMOS LMC660 amplifier ensured that the bias-current contribution would be less than 2 fA. By employing this technique, Grohe could simply remove any DUT (device under test), and the integrator would then have measured its own bias current as well as all the leakages from the test socket and the PCB on which the integrator was mounted.

Figure 7 shows that Grohe did not insert the DUT into a socket and that none of the pins are in contact with a PCB. To minimize leakage, Grohe brought up just two power pins as long, separate individual sockets that he did not mount to a PCB. Likewise, he hooked the pin to be tested to a socket and a 2-in. flying lead and connected that pin-and-socket combination to the integrating-amplifier input. To keep the DUT from running as an open loop, Grohe soldered together two sockets to bridge the output pins, which are suspended in air. Air currents can carry charged ions that can give false readings, so Grohe enclosed the entire DUT in a shielded copper-clad box.

The next issue was selecting an integrating capacitor. Initially, Grohe felt that the best capacitor would be an air-dielectric capacitor, so he fashioned two large plates, measuirng about 4×5 in., for the integrator capacitor. The size of this capacitor accounts for the size of the second copper-clad box on which the DUT box is mounted. Using a large capacitor proved to be a bad idea. The large area provides an ample target for cosmic radiation, creating ionized charges that interfere with the measurement (**Figure 8**). Grohe then minimizied the capacitor's size while still using a good dielectric. It occurred to him that RG188 coax cable uses Teflon insulation. A 2-in. section of this cable provided the 10 pF for the integration capacitor (**Figure 9**). As a further benefit, the outside braiding would serve as shield. Grohe therefore hooked it to the low-impedance-output side of the amplifier. With the switch to this capacitor, the cosmic rays struck only once every 30 seconds or so. Grohe took the integrated measurement for 15 seconds and, by taking five measurements, negated their effect. He then discarded any single outlying measurement. Any ionizing radiation sources, even an old watch with a radium dial, can cause cosmic-ray problems. Note that Grohe pried up the input pin of the amplifier to prevent leakage from the PCB.

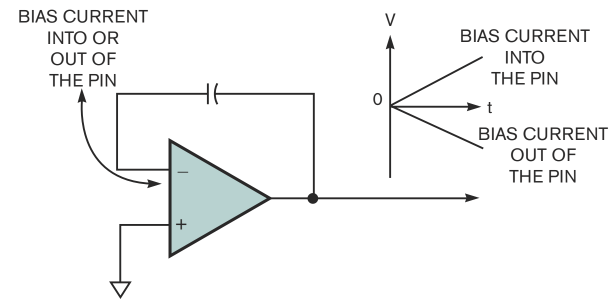

Figure 5 This integrator exemplifies the theory of using a capacitor in the feedback path of an amplifier to measure small currents.

Before taking a measurement, you need to reset the integrating capacitor to zero. Using a semiconductor switch is impractical, because of leakage currents and the 5- to 20-pF capacitance most analog switches offer. That capacitance exhibits the varactor effect, as well; it changes with applied voltage, further complicating measurement. To minimize these problems, Grohe used a Coto-reed relay. Knowing that the coil might couple to the internal reed when the relay was open, he specified a relay with an electrostatic shield. Much to his dismay, there still was a large jump in the measurement when the relay opened due to charge injection. It turns out that you can also look at a reed relay as a transformer, with the reed assembly representing a single turn. This phenomenon explains the failure of the electrostatic shield to prevent the interference. Magnetic fields inducing voltages in the high-impedance side of the circuit caused the charge injection.

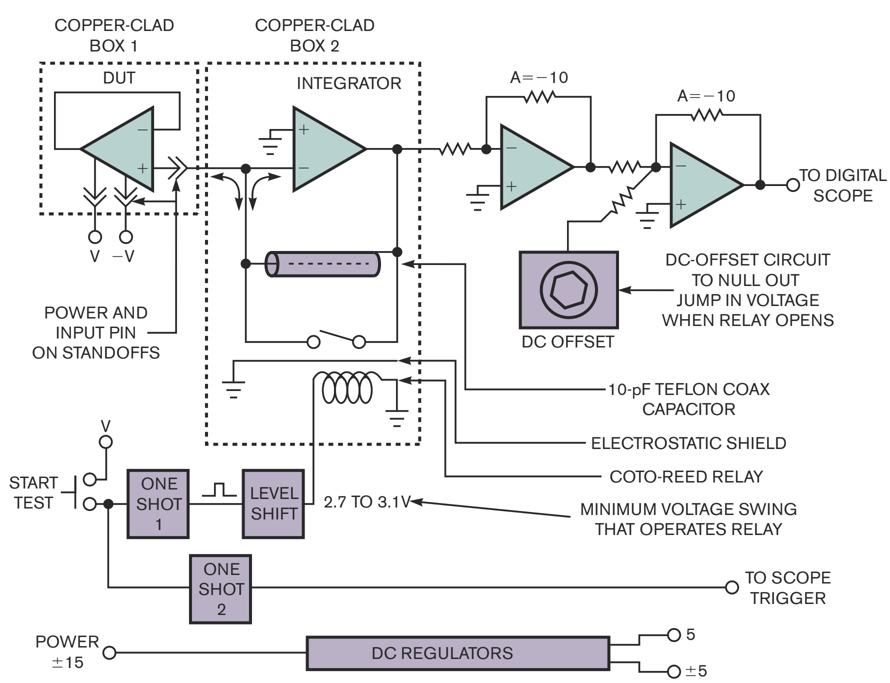

Figure 6 This circuit can resolve 1-fA bias currents coming out of the DUT.

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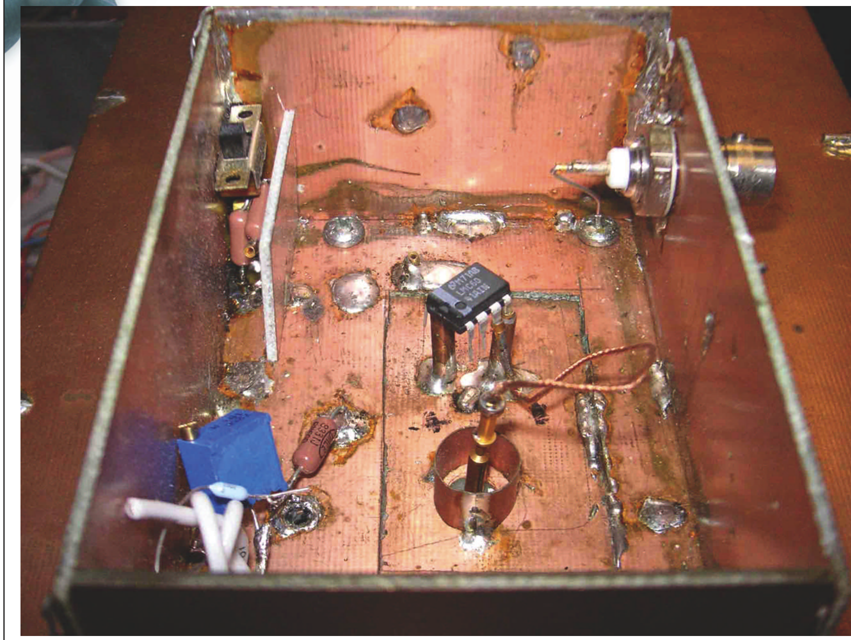

Figure 7 This configuration mounts the DUT on long standoffs that do not touch the PCB. Copper-clad boards serve as shielding (courtesy National Semiconductor).

The relay does not open instantaneously, and the pulse needed to energize the coil makes a significant current injection just before the relay opens. Grohe minimized this problem by characterizing the absolute minimum voltage swing needed to operate the relay he had installed. It turned out that the relay would pull in with 3.2V and drop out with 2.7V. He used a set of resistor taps on an LM317 adjustable regulator to control the output between these two values. By choosing not to energize the relay with a full 5V, he minimized the jump in the integrator output and made it repeatable. He then nulled out the jump by injecting a small current into the second gain-stage amplifier.

The gain stages are two low-noise amplifiers—the LMV751 or perhaps a chopper amplifier, such as the LM2011, would be suitable. Grohe sent this gained-up signal to a digital scope, which could record data and subtract the slope of the calibration run from the test runs to give a valid measurement. Grohe used two LS123-style one-shot circuits—one to trigger the relay and another to provide a suitable and repeatable time delay that triggered the digital scope.

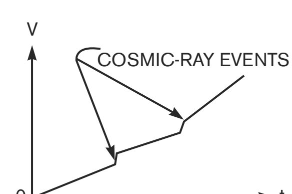

Figure 8 Cosmic rays impinge on the input node and capacitor, creating ions that make the measurement jump.

Grohe also understood that good low-noise-design principles also include the power rails to the parts, so he chose not to power the relay or digital circuits from the same power he used for the integrator and DUT. He used a handful of fixed and variable regulators to provide ±5V for the DUT and integrator, 8V for the relay-drive circuit, and a separate 5V for the digital circuits.

Using this circuit, Grohe was easily able to resolve 1 fA of current and found that most of the LMC6001 parts he tested had less than 5 fA of bias current, far exceeding the spec. He used this breadboard as the basis for a production-test circuit mounted on a standard probe card. (See **references 4**, **5**, and **6** for more about his design, including a video of the system.)

Grohe would not use this circuit to measure femtoampere currents in his lab. "I would wheel out the Keithley 2400 electrometer," he says. "We would have used that instrument to test the LMC6001 in manufacturing had the

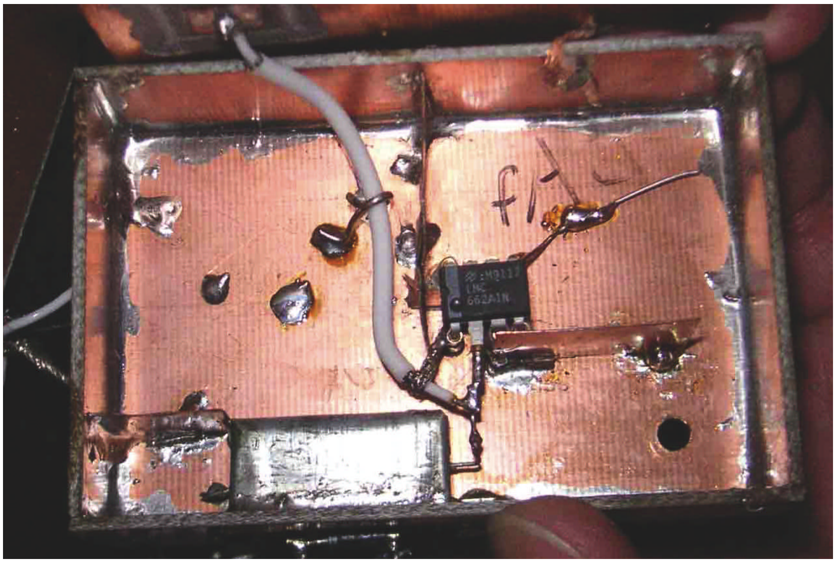

Figure 9 This copper-clad box mounts directly below the DUT box of Figure 7. Note the Teflon coaxial cable to create the integrating capacitor, as well as to provide a wire to bring the current to the input pin (courtesy National Semiconductor).

fab allowed us to use external test equipment." His faith in Keithley is well-placed. The company offers free on its Web site an excellent article on measuring attoamperes (**Reference 7**), as well as a book on delicate measurements (**Reference 8**).

DDC112

Grohe and Pease's integration approach is not limited to laboratory setups. Texas Instruments has created a line of parts that can measure in the femtoampere range and provide a digital output to boot. The line includes a single-channel DDC101 as well as the improved-sensitivity, dual-channel DDC112, which provides for external integrating capacitors. The four- and eight-channel DDC114 and DDC118 have a charge sensitivity of 12 pC (**Reference 9**). The sample rate for these 20-bit parts reaches 3 kHz.

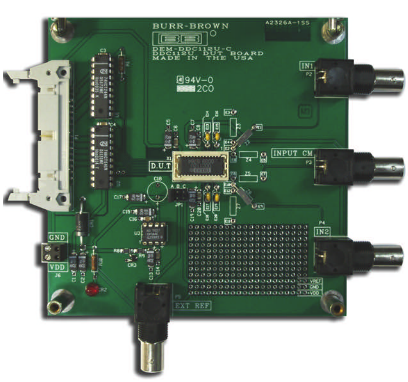

Figure 10 You can use this evaluation board for the DDC112 to measure femtoamperes of current. The DDC114 is even more sensitive (courtesy Texas Instruments).

You must be cognizant of physics to attempt these measurements. If the DDC112 can measure 12 pC of charge and you want to measure 12 pA of current, you need to set the integrating time to 1 second, the maximum the DDC114 allows. It is impossible to obtain a 3-kHz update rate if the part's integration interval is a full second. However, using the part configured in this fashion yields a 20-bit value at the end of the conversion. In other words, the DDC (direct digital converter) can resolve femtoampere currents, although at reduced accuracy. The input bias of the part is 20 fA, but your system's software can calibrate out this value, so the part should still be able to resolve to very low levels. Bear in mind that this type of sensitivity makes it difficult to calibrate the system just once in the factory and then have it work for all time. As temperature increases, the bias current increases, doubling every 10°C, and leakages as well as sensor drift can develop on your board. Providing the means for field calibration at power-up or more frequently is always a good idea

when measuring currents in the femtoampere range. Texas Instruments offers evaluation boards for these parts that you can get up and running in hours, measuring currents too small for even a good handheld digital voltmeter (**Figure 10**).

According to Jim Todsen, product-line manager for oversampling converters at TI and patent holder on the technology that the part uses, the DDC line's development started with the Burr-Brown ACF2101—a dual switched integrator front end that provides a single-chip option for the current-to-voltage function. The benefit of a dual integrator, Todsen explains, is that it is always collecting input current. While one integrator is sampling the input, the other side is presenting its integrated value to the ADC, and this process continues for as long as you need measurements. "After the ACF2101 converts the input current to a voltage," he says, "a discrete high-resolution ADC digitizes it. The DDC112 brought together both the current-to-voltage function of the ACF2101 and the digitization of the high-resolution ADC in one chip." He attributes this achievement to advances in wafer processing that allow high levels of mixed-signal integration as well as TI's development of a high-speed delta-sigma core that can provide the required speed and resolution to measure the front-end signals. "In addition," he notes, "we took advantage of having all the circuit elements under our control to optimize for very-low-leakage inputs and very stable performance over long integration periods."

These applications should convince you of the difficulty of measuring small currents. They should also convince you of the value of using proven parts and equipment—whether Analog Devices' AD549, National Semiconductor's LMC660, TI's DDC114 integrated circuits, Keithley's 2400 parameter-measurement unit, or Agilent's 4156 parameter-measurement unit—in this demanding application. Remember, though, that these remarkable parts and instruments are not magic boxes. You can take advantage of them only by removing noise sources and leakage paths from your board or test setup. Understanding op-amp specifications for voltage and current noise will help you select the right part (**Reference 10**). In the meantime, if your boss wants to know why you need $5 or $10 for a chip or thousands of dollars for an electrometer, you can now explain that, with the challenges entailed in measuring small currents, this equipment is a bargain. **EDN**

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BY CHENG PENG, PHD, AND THANH TRAN, PHD • TEXAS INSTRUMENTS

HD-video encoding with DSP and FPGA partitioning

IMPLEMENTING A SCALABLE VIDEO-ENCODING ARCHITECTURE THAT INCLUDES DSPs AND, WHEN NECESSARY, FPGAs AS COPROCESSORS TO OFFLOAD CERTAIN TASKS SATISFIES EVEN THE MOST DEMANDING VIDEO APPLICATIONS.

As video and imaging applications evolve toward high-definition compression standards, coprocessing architectures that include both DSPs and FPGAs are becoming popular. However, using partitioned systems is not the only option, because DSP architectures now include enhancements in performance, peripheral mix, video-hardware acceleration, and implementation techniques, and these advances have significantly broadened the range of applications in which DSPs can provide a complete approach.

DSPs have an inherent advantage because they are programmable, and their versatility allows designers to execute almost any algorithm. But when the computational load exponentially grows, as is the case with HD (high-definition) video, you can sometimes employ FPGAs to hard-wire certain computationally intensive tasks, thereby offloading the DSP. In video encoding, as in virtually all other engineering designs, no one-size-fits-all approaches exist. Even when you are employing a consistent codec, the end application plays a critical role in determining what level of computing power and memory bandwidth you require. These requirements, in turn, can play a dominant role in both hardware- and software-implementation strategies.

When dealing with compressed video, a standard compression algorithm is the most likely choice for experienced design teams. Once you select a codec, however, the next critical step is to assess the requirements of ME (motion estimation) and MC (motion compensation), because they can be two of the most demanding video-compression functions. Not surprisingly, the computational and memory bandwidth that the ME and MC engines demand depends on the amount of motion in the scene.

The H.264 AVC (advanced-video-coding) codec, for example, can find use in applications such as video surveillance, in which little action occurs over many hours of surveillance. At the other end of the spectrum, encoding HD video for a broadcast application can require a memory bandwidth of 20 Gbytes/sec or higher. HD videoconferencing, which might

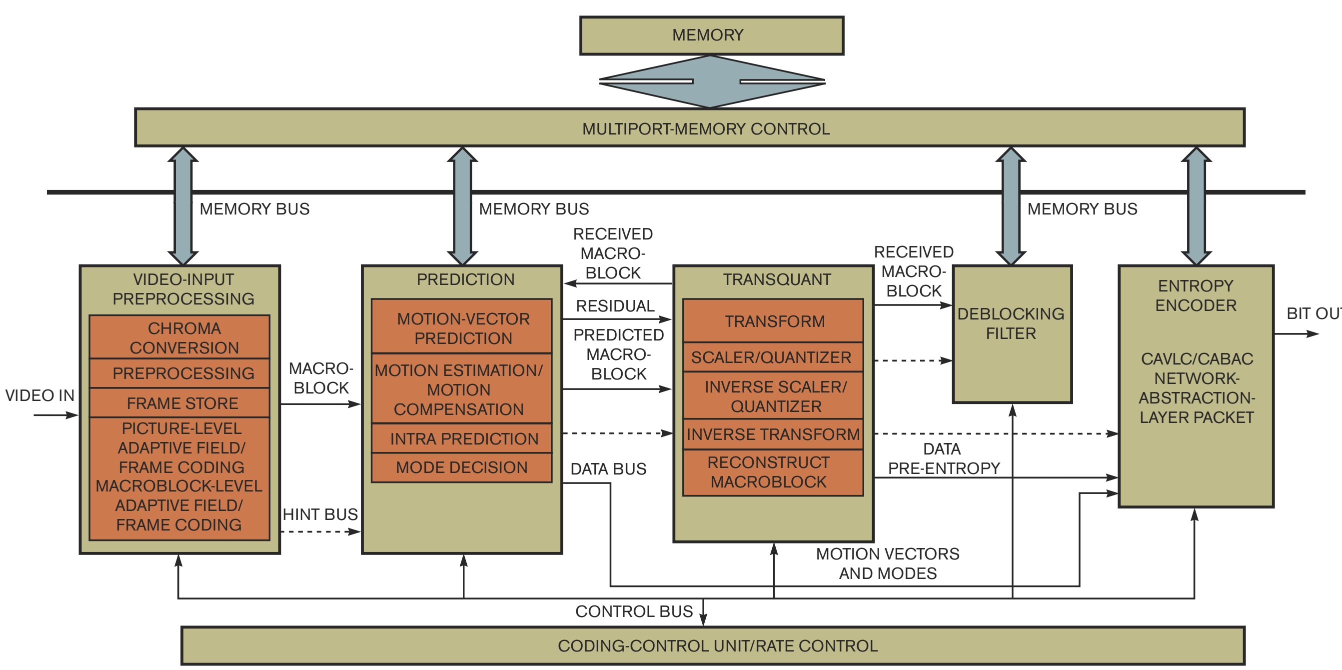

Figure 1 The encoder's motion-prediction block is critical to hardware partitioning.

require a memory bandwidth of 1.5 Gbytes/sec, lies between those extremes.

ENCODING HIGH-DEFINITION VIDEO

Although codec profiles go a long way toward creating a "packaged" approach for design engineers, the application has an impact equal to or higher than the codec on the implementation's hardware architecture. You can expect an HD-teleconferencing application, for example, to have relatively little frame-to-frame motion, but a broadcast-TV application must deal with the more intense video of sporting events, action movies, and other content in which you should expect a substantial amount of motion.

The ME and MC engines are key elements in a hardware-partitioning strategy, particularly for encoding video. The design team must consider whether they should implement only the ME engine on the FPGA or whether the computational load is heavy enough to require hardware acceleration of both the ME and the MC engines. The required memory bandwidth, which can be 20 Gbytes/sec or more, is just as important as the computational loading. FPGA-hardware architects may have flexibilities to scale the memory bandwidth as high as necessary and higher than the bandwidth that a DSP alone supports.

The H.264/AVC high profile is the obvious architecture for HD encoding of broadcast transmissions (**Figure 1**). For ME calculations, the current frame and each of the frames to which it will refer subdivide into macroblocks, which are typically 16×16 pixels in size but can be as small as 4×4 pixels. In a "matching" process, a search attempts to locate the macroblock in the reference frame that satisfies a predetermined minimum-error criterion from the current frame. The ME commonly uses the SAD (sum-of-absolute-differences) error criterion:

$$SAD=\sum_{i=0}^{15}\sum_{j=0}^{15}\left|x_y-y_y\right|,$$

where x is the current frame's macroblock, y is the reference frame's macroblock, and ij denotes the row (i) and column (j) of the frame. In some applications, the ME engine may have to calculate only 64 SADs per cycle, whereas, in others, it may have to execute thousands. The difference is significant, and, in high-end applications, it can lead to the use of architectures that either feature multiple DSPs or partition some of the calculations in a separate FPGA-based hard-wired accelerator.

Regardless of whether the FPGA is necessary to speedily calculate SADs or for its memory bandwidth, to be effective, it must have tightly coupled communication with the DSP. A macroblock-based pipeline-processing technique addresses this design challenge (**Figure 2**). The design should also reserve sufficient internal buffers to comprehend multiple macroblocks. While one macroblock is undergoing processing and a write to an internal buffer, the already-processed macroblock data in the other buffers can move to a subsequent processing unit.

In a synchronous design, it is important for the DSP and the

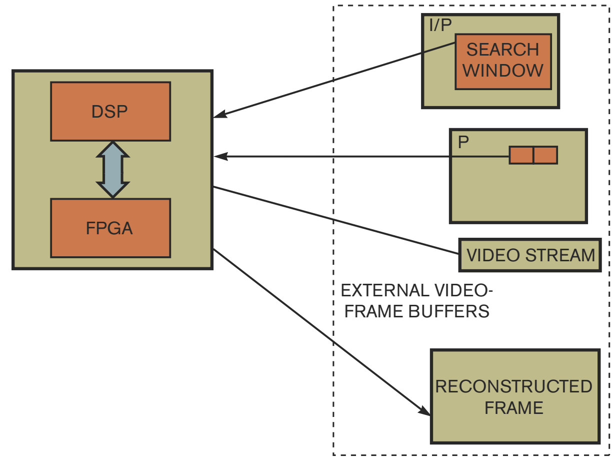

Figure 2 Macroblock-based pipeline processing encodes the P frame (middle) relative to the past reference frame. This reference frame can be either a P frame or an I frame (top). The past reference frame is the closest preceding reference frame.

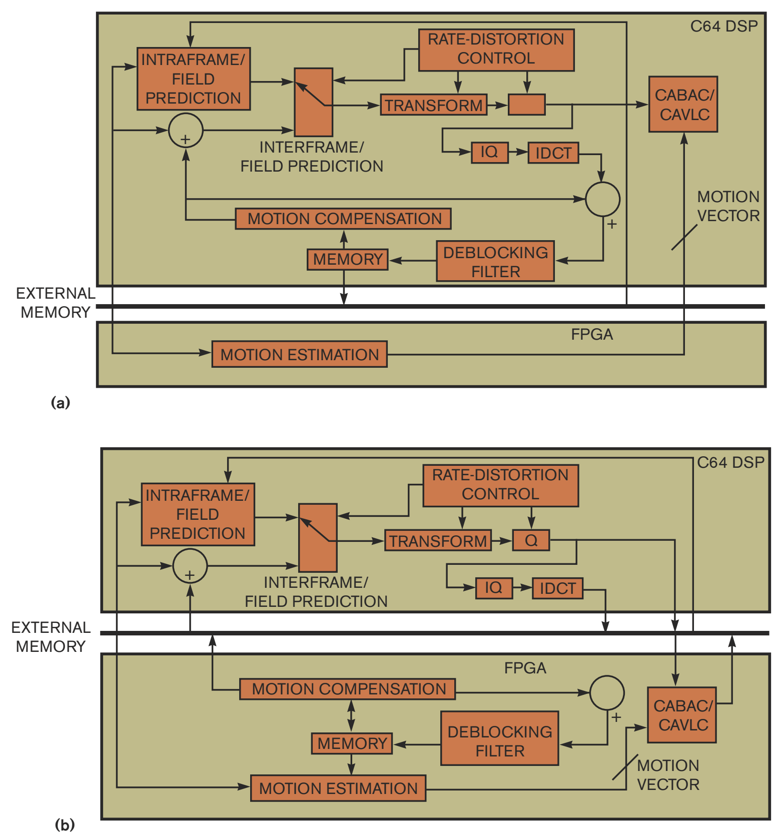

Figure 3 Executing motion compensation in the DSP requires only straightforward communication protocols (a), whereas the more FPGA-centric alternative approach increases the interactions between the DSP, the FPGA, and the system memory.

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PIC24FJ64GA008	80	64	
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PIC24FJ96GA006	64	96	
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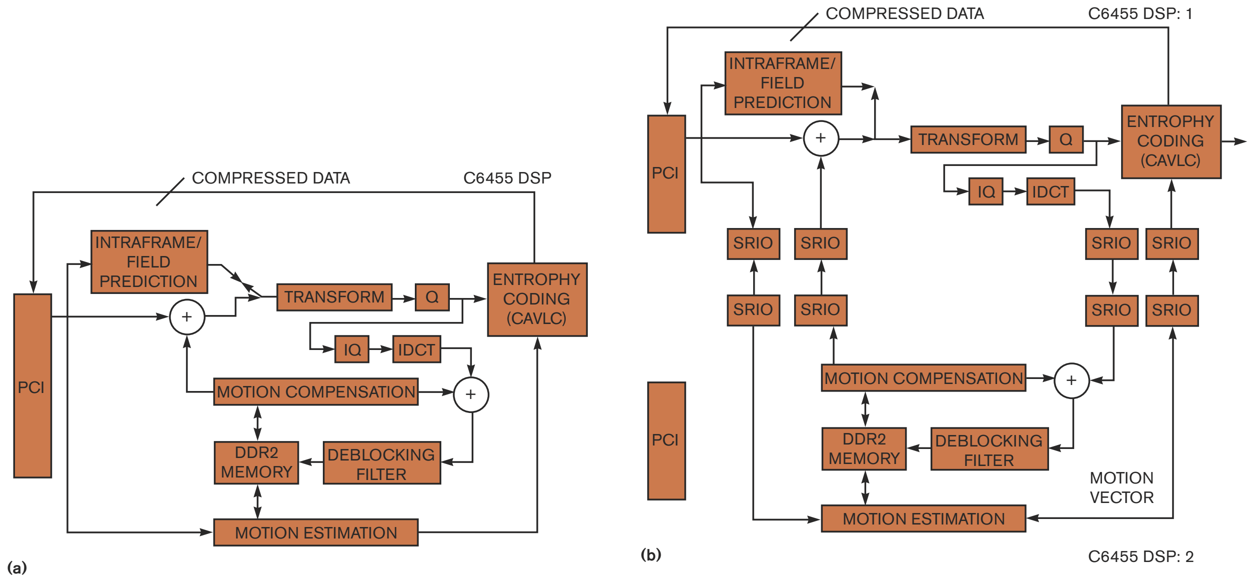

Figure 4 SD (a) and HD (b) encoding require, respectively, one and two 1-GHz DSPs.

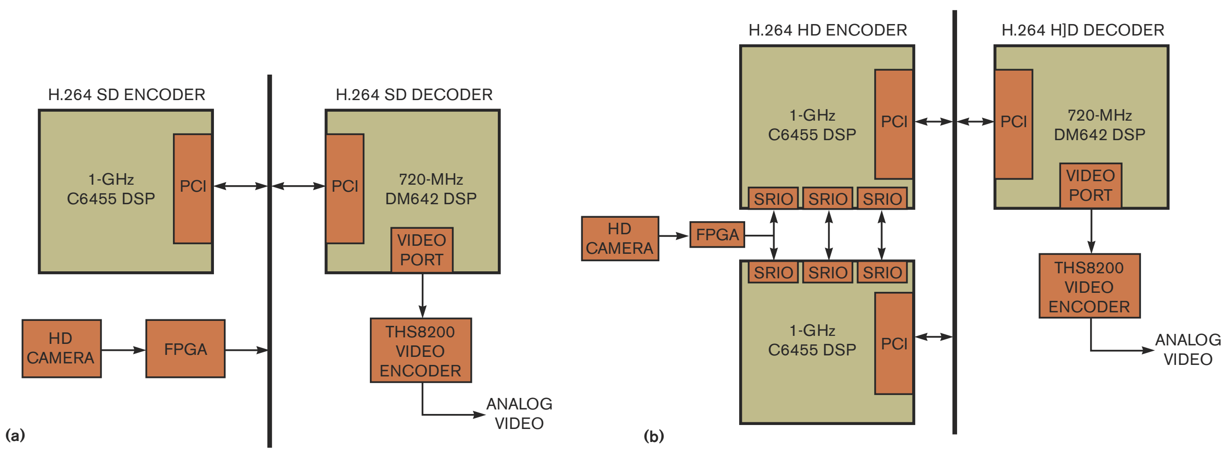

Figure 5 Simultaneous encoding-and-decoding applications at SD (a) and HD (b) resolutions supplement the encoding-only configurations with a 720-MHz media processor and an FPGA.

FPGA to access memory in a particular order and granularity, and it is important to minimize the number of clock cycles due to latency, bus contention, alignment issues, the DMA-transfer rate, and the types of incorporated memory. Interchip communication is equally critical in the implementation model (**Figure 3**). The architecture in **Figure 3a** implements only the ME engine on the FPGA, and the architecture in **Figure 3b** implements both the ME and the MC engines. Additional complexity in the MC case results from the fact that the ME engine and MC engine must continuously interact with each other. The architecture moves more than just the ME engine to the FPGA. The memory buffer, deblocking filter, and CABAC (context-adaptive-binary-arithmetic-coding) or CAVLC (context-adaptive-variable-length-coding) block also migrate from the DSP. CABAC compresses syntax elements in the video stream, and CAVLC, a less complex alternative, codes quantized transform-coefficient values.

The architecture in **Figure 3b** keeps a balance of functions between the DSP and the FPGA and enables both high performance and improved flexibility for H.264/AVC encoding. However, you should avoid using it whenever possible, because implementing memory-data transfers and communication protocols between the DSP and FPGA can be complex. The architecture in **Figure 3a**, conversely, often is a better choice because it simplifies memory-data transfers and the communication protocol between the DSP and the FPGA.

H.264/AVC ENCODING OF BROADCAST VIDEO

Broadcast-video encoding requires a different peripheral mix than with less demanding encoders in consumer devices' videoconferencing applications. High-end encoders must deliver high channel densities and throughput, along with a low cost per channel. The right mix of peripherals and memory go a long way toward reaching these goals. High-bandwidth peripherals are important in DSP- and FPGA-partitioning decisions and can allow designers to create high-performance applications by integrating multiple DSPs on a board. For instance, a 500-MHz DDR2 external-memory interface provides

twice the throughput of its lower speed DDR predecessor, allowing system designers to more quickly transfer data. The approach provides 2 Mbytes of L2 cache memory, enabling extra performance, further reducing the price per channel in infrastructure applications. And a gigabit Ethernet MAC (media-access controller) has 10 times the bandwidth of previous-generation devices.

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Using an SRIO (Serial Rapid input/output) bus on the DSP decreases overall system cost by reducing the need for additional devices for switching and processor aggregation. SRIO interconnect also enables high-speed, packet-switched, peer-to-peer connectivity, providing a performance breakthrough for multichannel implementations on multiple processors. A one-lane SRIO link is fast enough to send 1080i raw video between devices, and a four-lane SRIO link can easily shuttle 1080p raw video with bandwidth to spare. The use of SRIO in infrastructure applications with DSP farms can significantly cut system cost by reducing device count, board size, and per-device cost.

Although SRIO is not the only option that facilitates chip-to-chip connections, it delivers several advantages over traditional interchip connections, such as PCI and EMIF (External Memory Interface). SRIO achieves 1250-Mbyte/sec bandwidth versus 133 Mbytes/sec with PCI. In addition, SRIO directly supports message passing and multicast, which PCI does not support. SRIO also uses only 16 pins versus approximately 90 for EMIF and supports seamless connection with the master and slave interface, providing robust protocol and in-band interrupts.

The decreased bandwidth potential of traditional, non-SRIO interfaces may create the need for multiple parallel interfaces to achieve the required performance. Additionally, bus sharing by multiple devices can greatly reduce the I/O performance. Some interfaces can act as a master or a slave but not both, thereby requiring additional system support and glue logic. Traditional interfaces may also be physically unsuitable because they may consume too much PCB (printed-circuit-board) space due to wide parallel interfaces, or they may simply lack the needed advanced features, such as error detection and correction, status or acknowledgment feedback, or in-band-interrupt and -signaling functions.

SCALABLE SYSTEMS

Integrating high-bandwidth I/O blocks into a DSP has the expected result of adding another design option. With the availability of DSPs that can satisfy the memory bandwidth of real-time HD encoding of broadcast video, you should consider using multiple DSPs in most scenarios, instead of an inherently complex DSP-plus-FPGA combination. The primary motivation for using two DSPs for HD encoding is that chip designers have solved the interchip-communications problem for you. Scalability provides another DSP-centric motivation. Because the evolution to HD has only just begun, in many instances, designers find it useful to provide an SD (standard-definition) approach that they can scale to HD with little additional effort. Employing DSPs with high-

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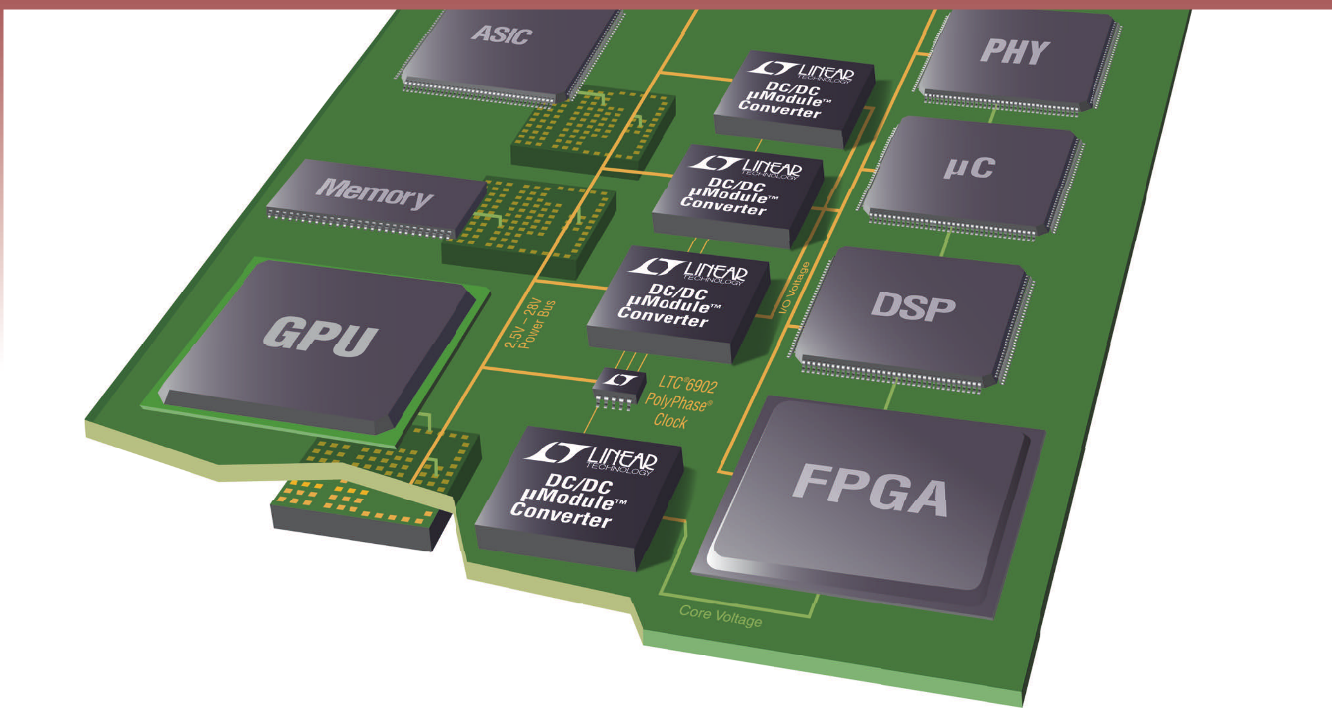

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LTM4603	6		✔	✔	✔		
LTM4603-1	6		✔	✔			
LTM4600	10						
LTM4601	12		✔	✔	✔		
LTM4601-1	12		✔	✔			
V_{IN}: 2.25V-5.5V; V_{OUT}: 0.8V-3.3V							
LTM4604*	4	2x for 8A	✔			2.3	9x15

*Future Product

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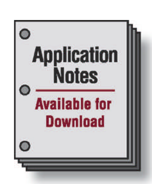

LINEAR TECHNOLOGY

performance I/O offers an easy migration path.

The starting point in this scalability strategy is encoding SD video. A 1-GHz DSP with a rich peripheral set can encode H.264/AVC's SD baseline profile at 720×480-pixel resolution and 30 frames/sec (**Figure 4**). Motion compensation executes on-chip. When the encoding requirement moves to HD—that is, 1280×720-pixel resolution at 30 frames/sec—you can employ two 1-GHz DSPs, with SRIO for interprocessor communication. ME and MC migrate from the chip that originally handled SD encoding to the second DSP. Note that neither of these designs requires FPGA assistance.

When the design scenario moves to an application requiring simultaneous encoding and decoding, you can still use DSPs to do most of the work (**Figure 5**). SD decoding on a 720-MHz media processor and encoding on a 1-GHz DSP benefit from the use of a separate FPGA to buffer the video from the camera. HD encoding and decoding employs fundamentally the same architecture as that of HD encoding but with the addition of the same low-cost, high-performance media processor and FPGA.

The HD system can perform simultaneous H.264/AVC, baseline profile, HD encoding, and HD decoding at 1280×720 pixels at 30 frames/sec. A DSP with SRIO provides chip-level interconnect and processor-to-processor communication at speeds as high as 10 Gbps with full duplex interconnectivity. In addition, using two or more DSPs with SRIO on the same board eases the implementation of multiprocessing architectures and ensures that no computing bottlenecks arise. A board with 10 of these DSPs, each clocking at 1 GHz and working in parallel, achieves 10-GHz performance. You can design the board to support multiple I/O modules, such as SRIO, HD SDI (serial-digital interface), and CameraLink.EDN

AUTHORS' BIOGRAPHIES

Cheng Peng, PhD, is a video-applications engineer at Texas Instruments, where he has worked for five years. He currently develops video-surveillance-over-Internet Protocol products. He focuses on video compression, including MPEG-2, MPEG-4, and H.264; HD-video implementation; and video intelligence, including motion detection, object tracking, and object recognition, using the TMS320C6000 DSP. He received a doctorate in electrical engineering from Texas A & M University (Galveston). He has published a book and several papers in the IEEE Journal.

Thanh Tran, PhD, is an embedded-systems manager at Texas Instruments, where he leads the hardware-systems team in developing reference designs and frameworks for high-speed DSPs and SOCs (systems on chips). He has extensive experience in audio-, video-, computer-, and communication-system design. He has a bachelor's degree in electrical engineering from the University of Illinois—Urbana/Champaign and master's and doctorate degrees in electrical engineering from the University of Houston. He has published more than 15 technical papers and holds 20 patents. He is also an adjunct faculty member at Rice University (Houston).

DESIGN NOTES

Micropower Op Amps Work Down to 1.8V Total Supply, Guaranteed over Temperature – Design Note 414

Glen Brisebois

Introduction

Micropower op amps extend the run time of battery-powered systems and reduce energy consumption in other energy limited systems. Nevertheless, battery voltages change as they are depleted. To maximize a system's run time, op amps should operate over a wide enough supply range to make use of the complete range of battery voltages, from fully charged to fully depleted. The new LT®6000 family of 1µA and 13µA op amps operates on supplies as high as 16V all the way down to 1.8V, guaranteed over temperature.

NiMH and Alkaline

A NiMH battery has a nominal cell voltage of 1.2V, but it depletes to 0.9V, below which the voltage rapidly falls off. The LT6000 family of op amps works directly from two series NiMH cells taking full advantage of their entire charge discharge cycle. Likewise, an alkaline battery has a nominal cell voltage of 1.5V, but can deliver energy down to depletion levels of a few hundred millivolts. So, the LT6000 can happily operate from two series alkaline cells, and just as well operate directly from a 9V alkaline battery (6 series cells) from full charge all the way down to very extreme depletions (300mV average cell voltage for 1.8V total). Sure, other low voltage op amps can operate at the depleted end of this battery range, but few of those can also tolerate a 9V supply.

Supply Friendliness

Some micropower op amps have annoying properties such as drawing excessive current at start-up (commonly called carrots) or when the output hits a supply rail. These current spikes defeat the purpose of the micropower operation by hastening battery discharge. Worse yet, they may altogether prevent the supply from coming up in the case of a current limited supply, effectively crowbarring the system. Figure 1 shows the LT6000 and LT6003 supply current vs applied supply voltage at various temperatures. The LT6000 family eliminates carrots or at least chews them down to stumps.

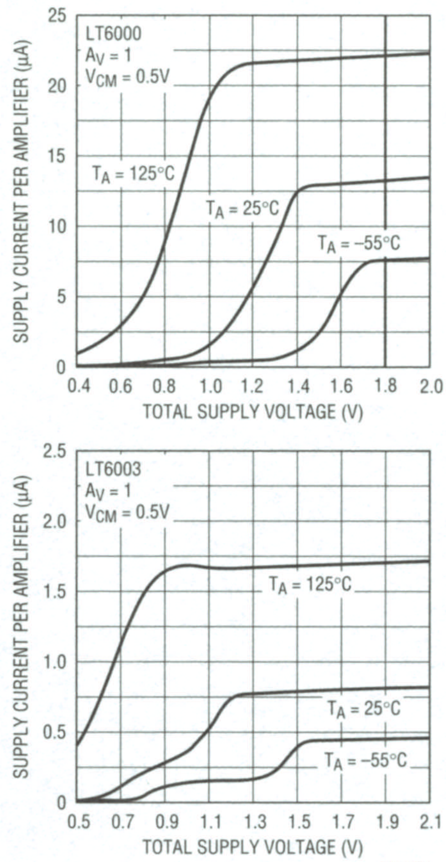

Figure 1. Clean Start-Up Characteristics Without Current Spikes

Portable Gas Sensor

Figure 2 shows the LT6003 applied as an oxygen sensor amplifier. The oxygen sensor acts much like an air powered battery, and generates 100µA in one atmosphere of fresh air (20.9% oxygen). It is designed to operate into a 100Ω resistor, for a 10mV full-scale reading. The op amp amplifies this voltage with a gain of 100 as shown (101 actually), for a 1V full-scale output. In terms of

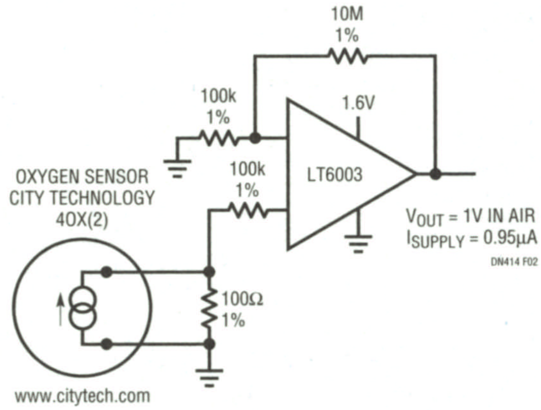

Figure 2. Micropower Oxygen Sensor

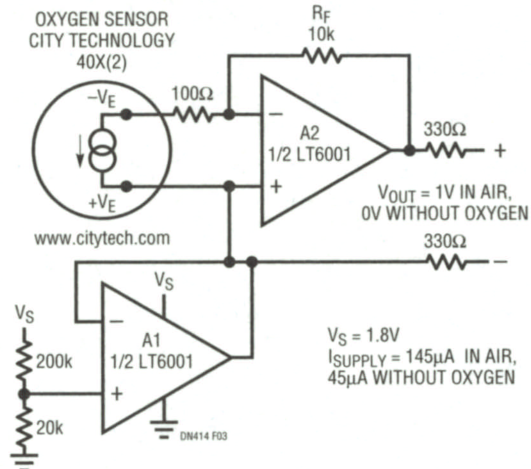

Figure 3. High Accuracy Oxygen Sensor

monitoring environments for adequate human-livable oxygen levels, 18% oxygen content translates to an output voltage of 0.86V. Oxygen contents below this are considered hazardous. Oxygen deprivation in the lungs causes immediate loss of consciousness and bears no resemblance to holding your breath. Total supply current for the circuit is 950nA. The 500μV worst-case input offset voltage at room temperature contributes a 50mV uncertainty in the output reading.

Better low value accuracy can be obtained by implementing a transimpedance approach as shown in Figure 3. Op amp A1 provides a buffered reference voltage so the circuit is accurate all the way down to a zero-oxygen environment without clipping at ground. Op amp A2 provides the current-to-voltage function through feedback resistor R_F. The sensor still sees the 100Ω termination, as the manufacturer specifies. The output voltage is still 1V in normal atmosphere, but note that the noise gain is not much higher than unity so the output error due to offset is now 500μV worst case instead of the 50mV of the previous circuit. This considerable improvement in accuracy exacts some price in supply current, because the oxygen sensor current is now provided back through R_F by the op amp output, which necessarily takes it from the supply. The supply current is therefore oxygen-presence dependant. Nevertheless, this solution is still ultralow power when monitoring environments that are oxygen-free by design, such as environments for food storage and those designed to inhibit combustion. It would also be ideal for portable sensors where the detected substance is not oxygen but is rather a hostile substance, which is not normally present and is therefore usually low current.

Conclusion

The LT6000 and LT6003 family of op amps offer 13μA and 1μA micropower operation over a wide supply range from 18V all the way down to 1.8V, guaranteed over temperature. Careful attention was paid during the design phase to minimizing gotchas such as supply current carrots. They are ideal for maximizing battery life in portable applications, operating over a wide range of battery charge levels and environments.

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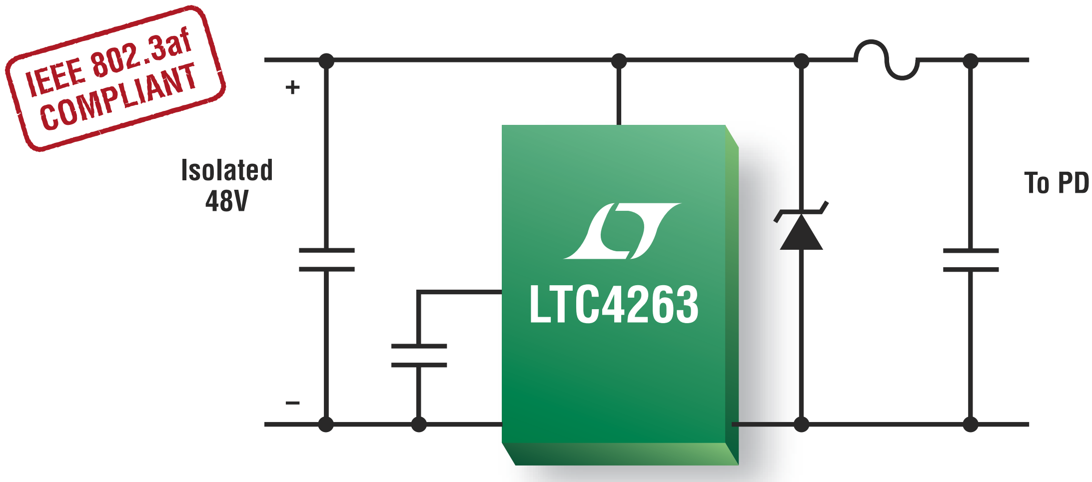
Single Port PoE



Fully Autonomous Controller with Integrated FET Simplifies PSE Design

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Features

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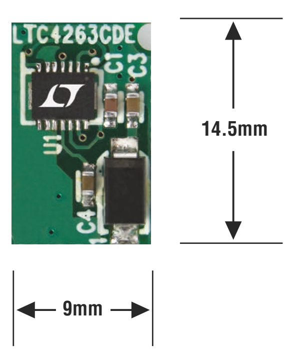
- LTC4263: $2.95 each in 1k qty

Small Footprint, Simple Design



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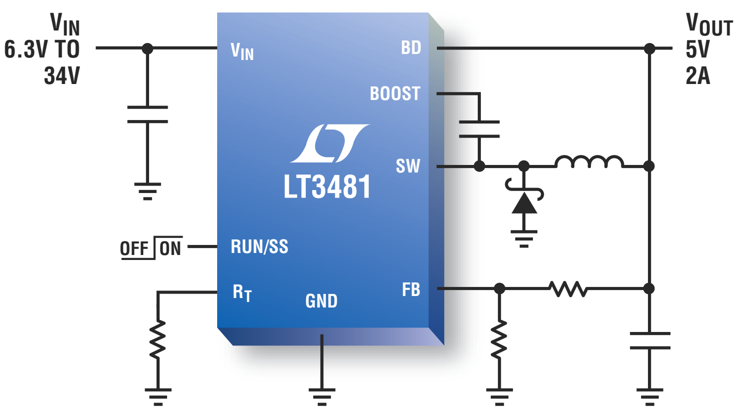
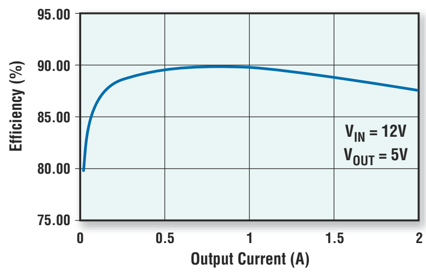
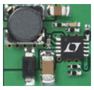
36V Buck Converter Has It All



Efficiency vs Output Current





Actual Size Demo Board

2A Output Current, 50µA Quiescent, 2.8MHz Switching in 3mm x 3mm DFN

The LT®3481 monolithic buck converter has everything needed to simplify mid-range input voltage step-down conversion designs. Its high switching frequency operation minimizes the size and cost of capacitors and inductor. Low ripple Burst Mode® operation typically has less than 15mV$_{P-P}$ ripple at the output and a quiescent current of only 50µA. The internal 3.2A rated switch provides 2A of continuous output current at voltages as low as 1.27V. With its high level of integration and fast switching, a complete LT3481 solution occupies less than 1cm^2.

Features

- Input Range: 3.6V to 36V (Max.)
- 2A Maximum Output Current
- Low Ripple Burst Mode Operation
  50µA at 12V_{IN} to 3.3V_{OUT}
  Output Ripple < 15mV
- Adjustable Switching Frequency: 300kHz to 2.8MHz
- Integrated Boost Diode
- Small 10-Pin Thermally Enhanced MSOP & 3mm x 3mm DFN Packages

Low Output Ripple

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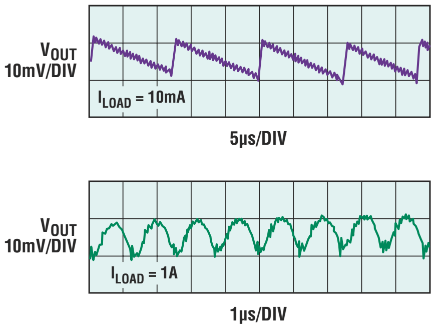

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Use a CFL ballast to drive LEDs

Christian Rausch, Unterhaching, Germany

Designers use ballast ICs, such as International Rectifier's (www.irf.com) IR53HD420, in CFLs (compact fluorescent lamps) for heating the filaments, igniting the lamps, and supplying the lamps with current (**Reference 1**). Manufacturers produce these ICs in high volumes, and they cost approximately $2. This Design Idea shows how you can use a CFL-ballast IC for driving LEDs instead of CFLs. A ballast IC essentially is a self-oscillating half-bridge for offline operation. It typically operates from 320V dc, which is approximately the same power as that from a 230V-ac mains rectifier or a 120V voltage doubler. The IC generates square-wave voltages with an amplitude of 320V p-p and a frequency of tens of kilohertz.

Usually, this square-wave voltage connects to a series combination of a CFL tube and a current-limiting inductor, L_1 (**Figure 1**). Together with a parallel capacitor and using the LC resonance, you can warm up, ignite, and supply the tube with current. This approach works well because CFL tubes have high impedances when they are off and low impedance when they are running. The tube voltage is typically 150V p-p.

By putting several LEDs in series and connecting them to a bridge rectifier, you can effect an imitation of a CFL, at least in the on-state. Imitating the off-state is less important, because LEDs need no ignition procedure. At the given values for R_T and C_T, the bridge runs at 70 kHz. The circuit supplies 64 LEDs with a current of approximately 80 mA. The infrared LEDs illuminate the field of view of a CCD camera in a machine-vision system. The circuit prototype uses a 2.7-mH inductor from a dead CFL.

The LED current comprises dc current plus a small ripple current; keep

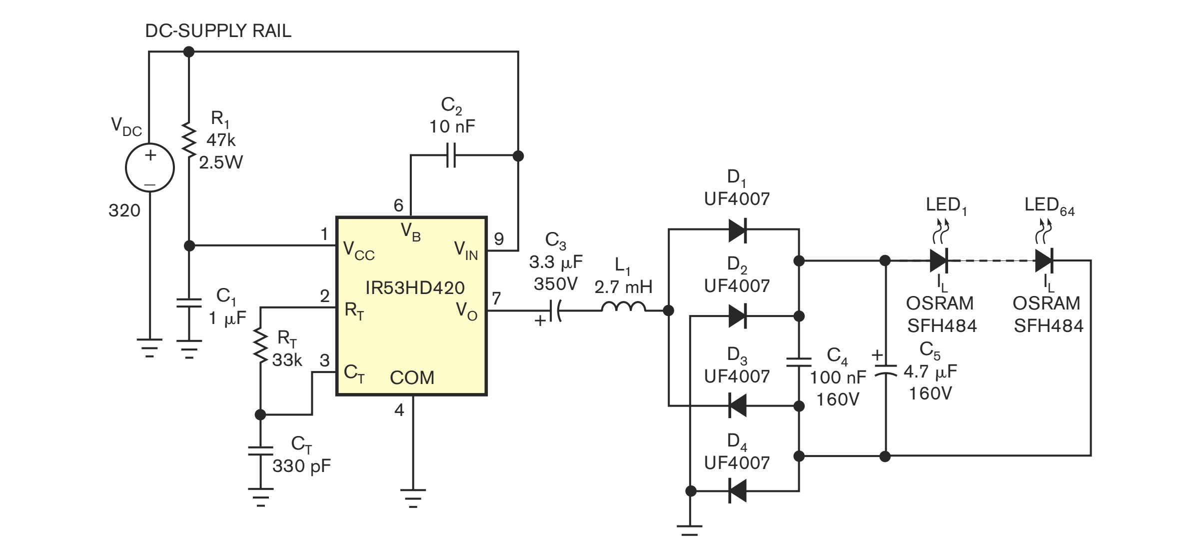

Figure 1 A CFL ballast drives a long string of LEDs.

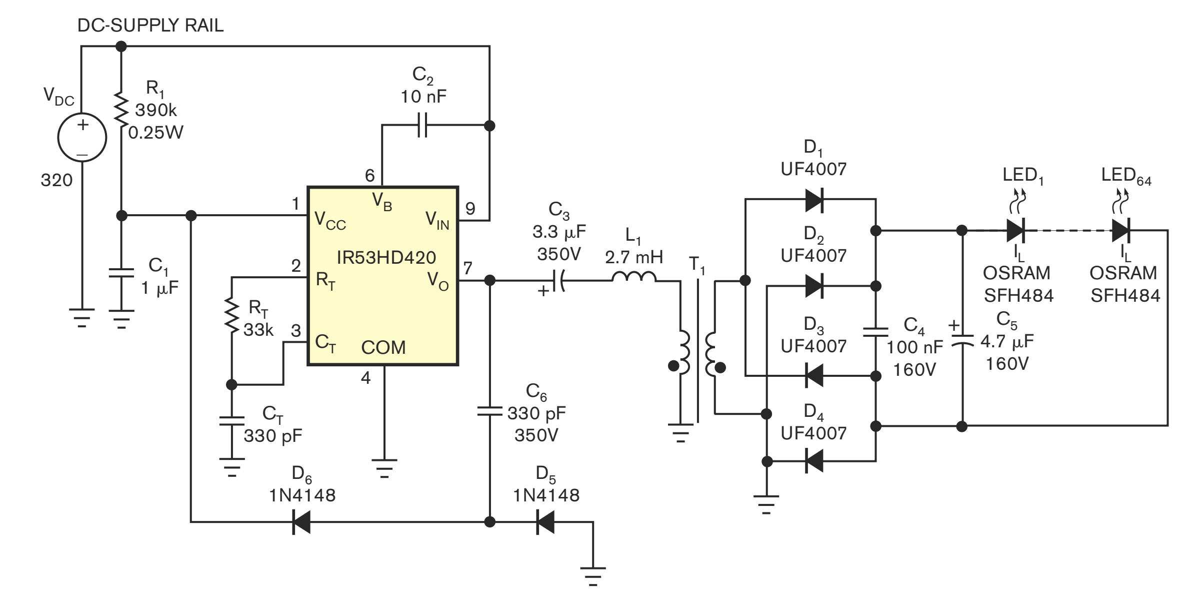

Figure 2 Adding a transformer to the circuit of Figure 1 allows you to connect as many LEDs as necessary.

the ripple current low for high efficiency and long LED lifetime. LED manufacturers usually demand values of a few percentage points. Such a low ripple current may be difficult to achieve with one electrolytic capacitor, C_5, but a parallel combination with an additional foil capacitor, C_4, works well enough in most cases. The voltage at the input of the LED rectifier is fairly constant during one oscillation period, so the inductor current has a triangular shape, which is good for EMC (electromagnetic compatibility). The equation for the average LED current is $I_{LEDAVG}=(½\times V_{DC}-N\times V_{FLED})/(4\times f\times L_1)$, where V_{DC} is the supply voltage, N is the number of LEDs in series, V_{FLED} is the LED forward voltage, f is the oscillation frequency, and L_1 is the inductance of the current-limiting inductor.

Although the circuit of **Figure 1** works well, it has some deficiencies that the circuit of **Figure 2** remedies by adding C_6, D_5, D_6, and T_1, wound on an EPCOS EP13 coil former, with an ungapped-EP13-core of T38 material with an inductance of 7000 nH. Both the primary and the secondary windings are 90 turns of 0.2-mm wire; the secondary winding is wound on top of the primary winding. Stray inductance is not important in this case, and the inductance for both the primary and the secondary windings is 50 mH. The circuit in **Figure 2** has several advantages over the one in **Figure 1**. For example, the supply current for the ballast IC of **Figure 1** must flow through R_1 and into the IR53HD420, where it gets clamped to 15.6V. At a supply current of about 6 mA, R_1 must dissipate more than 2W. In **Figure 2**, R_1 can have a much higher value, because it must supply only a small start-up current. After start-up, a charge pump comprising C_6, D_5, and D_6 pumps enough current into the V_{CC} pin so that the internal zener diode clamps to 15.6V. The design equation for the charge pump is $I_{SUPPLY(AVG)}=f\times C_6 2\times V_{DC}-15.6V$. The dissipation of R_1 now stays below 0.25W.

WITH THE TRANSFORMER, YOU CAN GROUND ONE END OF THE LED STRING EITHER DIRECTLY OR THROUGH A CAPACITOR.

Also, the summed forward voltages of the LEDs in **Figure 1** must be smaller than one-half the supply voltage. For the circuit in **Figure 2**, by tailoring the transformer-winding ratio, you can connect as many LEDs as needed, as long as you do not exceed the ratings of the components. (LED voltages even higher than V_{DC} are possible.) A less obvious problem of the circuit in **Figure 1** is that the full voltage swing of the bridge appears at both ends of the LED string. This situation does not present a problem when all the LEDs are close together and the LEDs are close to the bridge. However, in many light fixtures, you wish to separate the LEDs from the electronics. Due to stray capacitances, this approach would lead to high capacitive currents from the LEDs to ground, corrupting the efficiency and producing EMC problems. With the transformer of **Figure 2**, you can ground one end of the LED string either directly, as shown, or through a capacitor. Now, you can use long cables to easily separate the LEDs from the electronics.EDN

REFERENCE

1 "IR53H420(D)420, Self-Oscillating Half Bridge," Preliminary Data Sheet No. PD60140-K, International Rectifier, Aug 19, 2003, www.irf.com/product-info/datasheets/data/ir53h420.pdf.

Photodiode amplifier exhibits one-third the output noise of conventional transimpedance amp

Glen Brisebois, Linear Technology Corp, Milpitas, CA

A conventional 1-MΩ transimpedance amplifier has at least 130 nV/√Hz of output-noise density at room temperature (**Figure 1**). You can consider the 130 nV as the theoretical noise floor limit of the amplifier because that is the noise density of the 1-MΩ resistor itself. Any noise in the op amp can only make things worse. Cooling the resistor to 77.2K, the temperature of liquid nitrogen, quiets it to 65 nV/√Hz, provided that it survives, but is that the only option? Can you beat the 130-nV theoretical noise floor without cooling?

Figure 2 shows one way. IC_1, a Linear Technology (www.linear.com) LTC6240, provides an overall transimpedance gain of 1 MΩ, but it has an output-noise density of only 43 nV/√Hz, about one-third of a conventional 1-MΩ transimpedance amplifier at room temperature. It achieves this figure by taking an initial transimpedance gain of 10 MΩ and then attenuating by a factor of 10. The transistor section provides voltage gain and works on a 54V supply voltage to guarantee adequate output swing. By achieving an output swing of 50V before attenuation, the circuit maintains an output swing to 5V after attenuation. The 10-MΩ resistor sets the gain of the transimpedance-amplifier stage and has a noise density of 400 nV/√Hz. After attenuation, the amplifier's effective gain drops to 1 MΩ, and the noise floor drops to 40 nV/√Hz, which dominates the observed 43 nV/√Hz. To achieve this noise performance by cooling requires a temperature of 33K, much colder than liquid nitrogen. Note also that the additional benefit of this method is that it divides the offset voltage of the op amp by 10. The worst-case output offset for this circuit is 105 μV over temperature. Bandwidth is 28 kHz. **EDN**

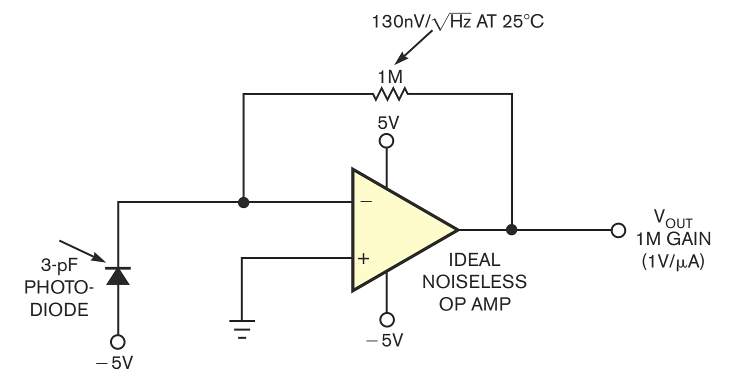

Figure 1 A conventional 1-MΩ transimpedance amplifier exhibits 130 nV/√Hz of output noise, even with a noiseless op amp. Cooling the resistor reduces the noise, but can you do better without cooling?

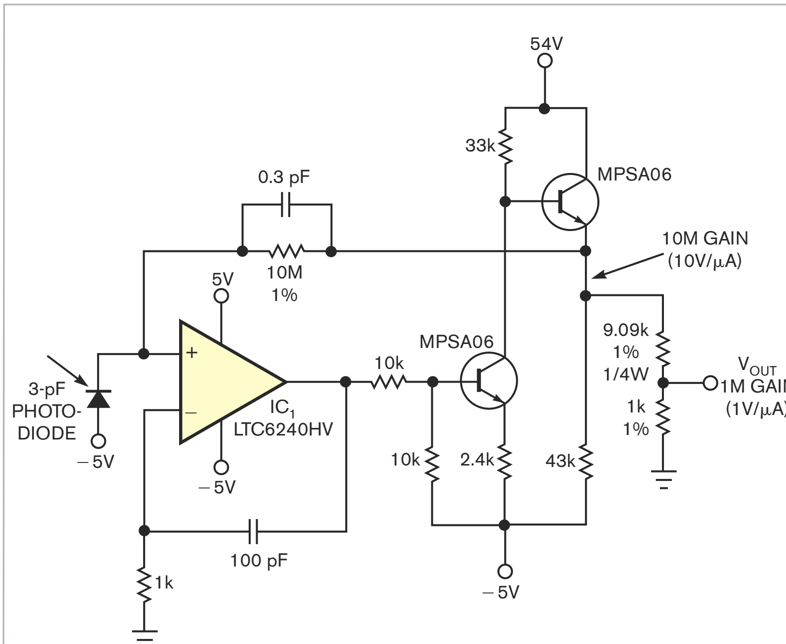

Figure 2 This effective 1-MΩ transimpedance amplifier has only 43 nV/√Hz of output noise. The circuit takes 10 times the high amplifier gain and then attenuates by a factor of 10. The LTC6240 has low current and voltage noise. The discretes allow for high output swing at the 10-MΩ gain node, so that a 0 to 5V output swing remains after attenuation.

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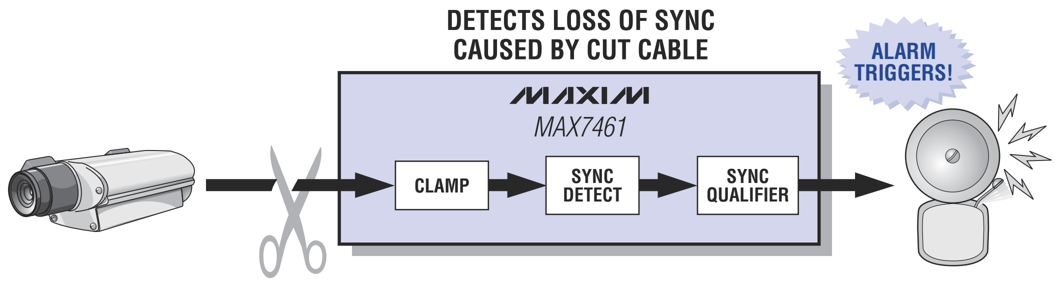

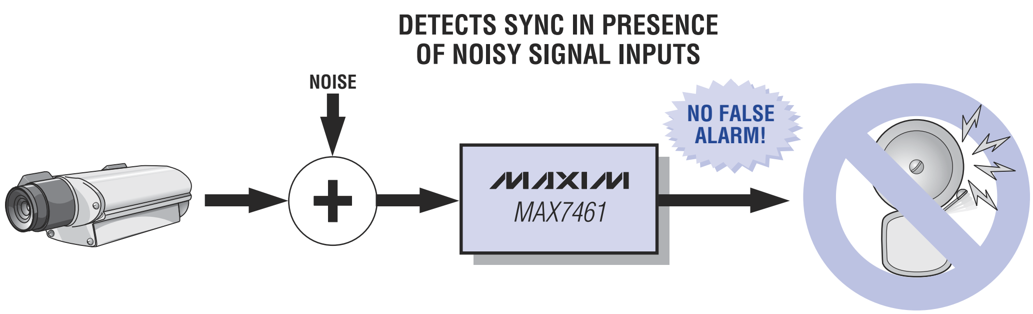

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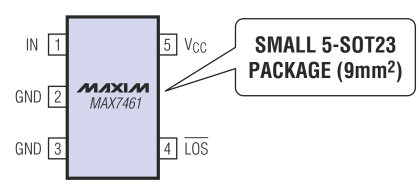

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Microcontroller programmer taps power from PC's serial port

GY Xu, XuMicro, Houston, TX

Just like a PC's USB port, the serial port on a PC can also in some cases serve as a power supply. A USB port can provide as much as 500 mA at 5V, but a serial port provides less power. Even with the serial port's limited capacity, serial-port power can still be a convenient power source for today's electronics. One obvious example is to light up an LED. **Figure 1** shows a simple way to tap the serial port's power. Under Windows XP, this task requires appropriate software. You can download the **listings** for this Design Idea from www.edn.com/070426di and run the program pwon.exe for this demo.

A far more useful case is to provide a power supply for the microcontroller programmer, which has no wall wart. Today's microcontrollers consume less current than their predecessors, so you can easily tap the serial port's power for an Atmel (www.atmel.com) AVR programmer (**Figure 2**). The programmer uses only two chips: IC_1, a Maxim (www.maxim-ic.com) DS275 for the RS-232 interface between the programmer and the PC, and IC_2, an Atmel AT89C2051 firmware microcontroller, which is the heart of programmer and handles all programming chores and communications with the PC. IC_3 is the AVR microcontroller, an AT90S1200/2313. You can also substitute an eight-pin AT90S2323/2343 or a 40-pin AT90S4414/8515. The SPI (serial-peripheral-interface) bus performs the device programming.

The basic requirement is that the circuit's total current consumption must be less than 10 mA. The programmer uses two RS-232 pins: DTR (data-terminal ready) and RTS (request to send) as a minuscule power source. The

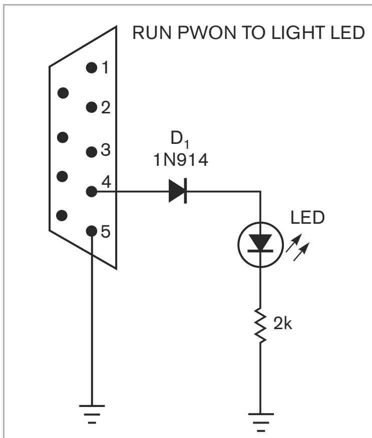


Figure 1 With the aid of a simple PC program, you can tap a PC's serial port for enough power to light an LED.

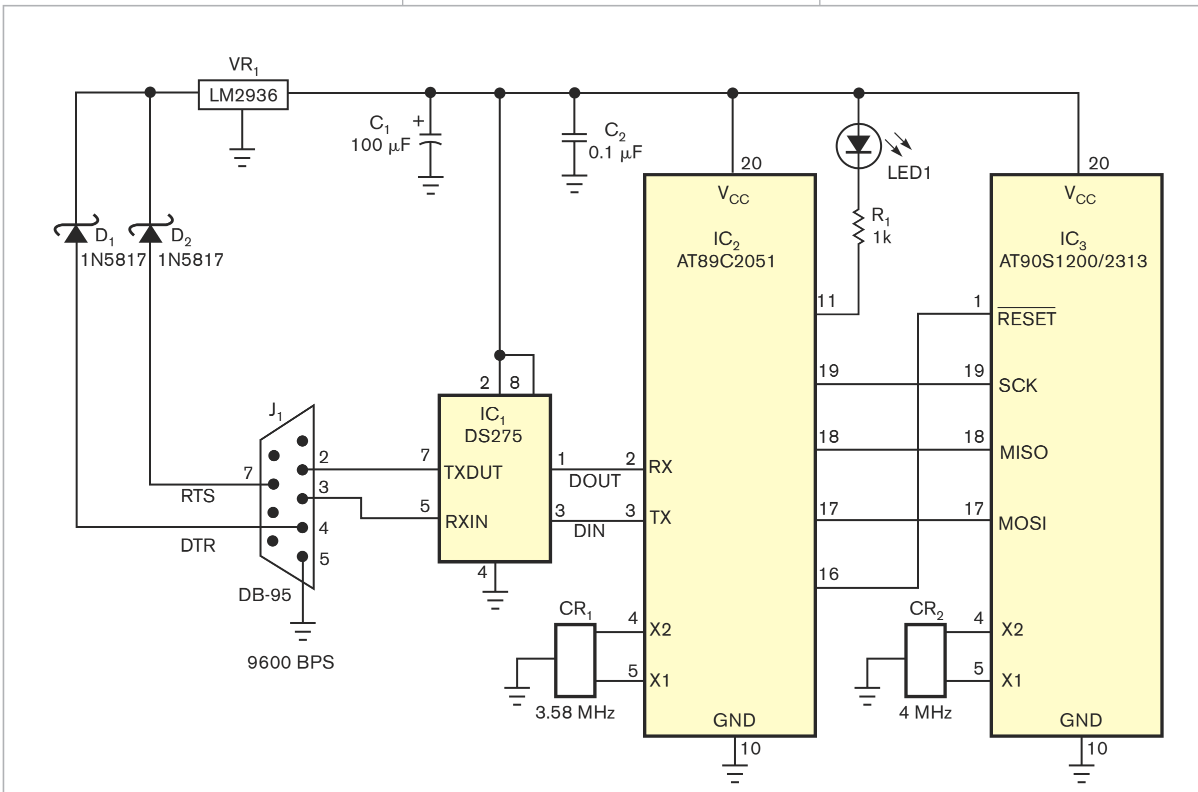
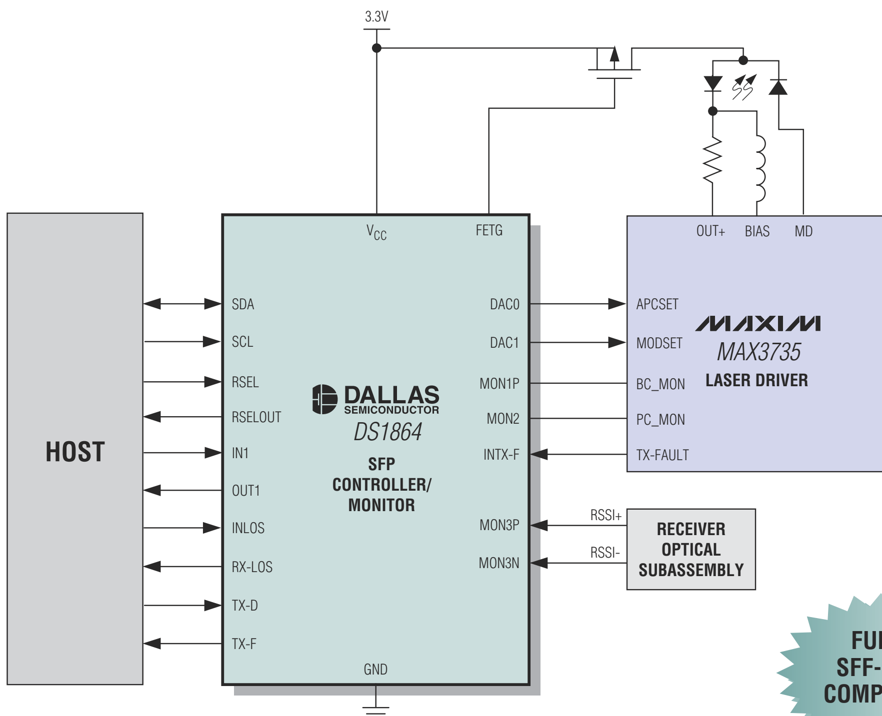


Figure 2 This microcontroller programmer gets its power from the PC's serial port.

COMPLETE SFP CONTROLLER/MONITOR SIMPLIFIES SFP MODULE DESIGN

Integrates All Functions Required for Controlling and Monitoring SFP Transceiver Modules

The DS1864 controls laser-driver bias/modulation currents and provides all the system monitoring functions and memory required for SFP optical transceivers. This device simplifies SFP module design, while providing the highest performance control and monitoring functionality.



FULLY SFF-8472 COMPLIANT

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- Fulfills All SFF-8472 MSA Requirements
  - Integrated 12-Bit ADC Monitors Temperature, V_{CC}, and Three External Analog Channels
  - Provides A0h and A2h EEPROM
- Integrates Laser-Shutdown and Eye-Safety Features
- I²C-Compatible Serial Interface
- 28-Pin, 5mm x 5mm TQFN Package

outputs from these pins arrive at a pair of Schottky diodes, D_1 and D_2, which cause a forward-voltage drop of only 0.3V, and then to VR_1, an LM2936 low-dropout-voltage regulator. Capacitors C_1 and C_2 smooth the output voltage. To reduce current consumption, LED_1 uses a 1-kW current-limiting resistor, and the control firmware turns it on only after the programming task completes; otherwise, LED_1 is off.

The circuit for the programmer is easy to build. The 8051-like AT89C2051 has 2 kbytes of flash program memory. It needs no components connected to the reset (Pin 1), and it uses the 3.58-MHz ceramic resonator to generate 9600 bps for communication with the host PC. In addition to eliminating an external power supply, the programmer needs only firmware design. The programmer uses the Windows HyperTerminal program to communicate with the programmer firmware. You configure the HyperTerminal to use a COM port with 9600 bps and set the flow-control parameter to XON/XOFF.

You can program the firmware files in **Listing 1** into the AT89C2051 using any 8051 programmer, and the **listing** includes one AVR sample demo file to program into the AT90S1200/2313. EDN

Circuit charges supercapacitors to 7V from USB power

Fran Hoffart, Linear Technology, Santa Clara, CA

Charging a supercapacitor from a 5V USB port may seem simple at first, but to charge three supercapacitors to 7V and to limit the input current to the 500 mA maximum limit on the USB port is somewhat more difficult. The circuit in this Design Idea uses a Linear Technology (www.linear.com) LTC3458 switching regulator to charge three series-connected supercapacitors and provide input-current limiting. This regulator limits the input current, as the capacitors charge, to less than 500 mA to satisfy USB specifications, and it provides the boost function to charge the capacitor to a voltage greater than the 5V USB input. Once the supercapacitor charges, the regulator maintains 7V at the output and can supply a continuous load of approximately 300 mA in addition to brief current surges of several amperes without exceeding 500 mA at the input. Typical loads requiring high surge current can include motors when initially starting up.

Removing the input voltage shuts down the regulator and reduces the capacitors' discharge current to approximately 3 μA, essentially the current through the voltage programming resistors. Manual shutdown is also possible by pulling the shutdown pin low, but, with the input voltage still applied, the capacitors' discharge current increases to approximately 30 μA. The circuit in **Figure 1** is programmed for a switching frequency of 1 MHz with an output voltage of 7V. A resistor on

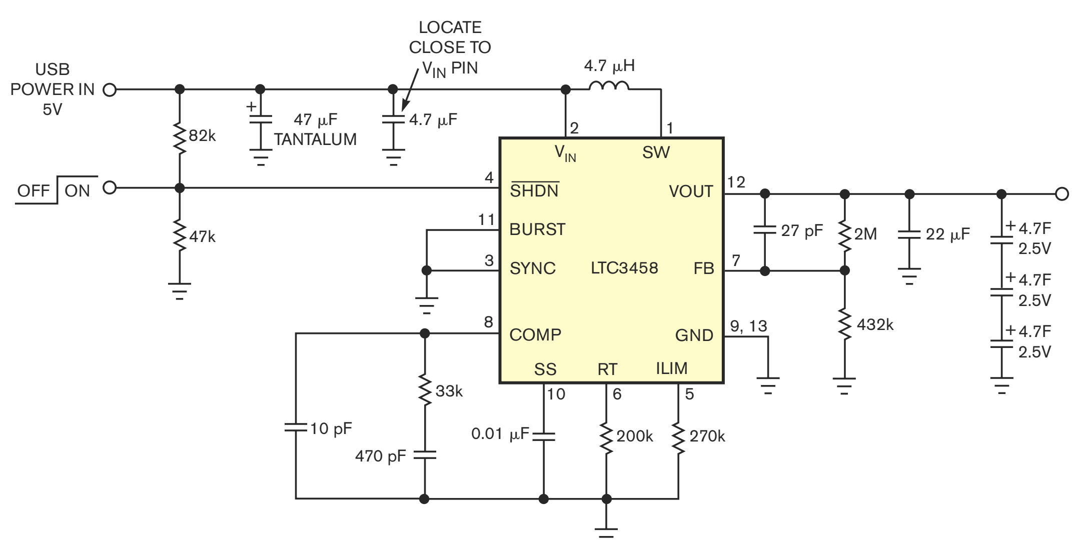

Figure 1 This circuit has a switching frequency of 1 MHz and an output voltage of 7V.

Low-Power DACs in Miniature Packages

8-/10-/12-Bit D/A Converters Provide Seamless Upgradeability

Features

- Pin- and function-compatible across resolutions
- 2- and 4-channel family with smallest package outline in-class (3 mm x 3 mm LLP)
- Rail-to-rail output swing
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  2 channel, 270 µA (max)
  4 channel, 485 µA (max)
- External reference (2- and 4-channel)
- Accepts input clock rates up to 30 MHz over 2.7V to 5.5V
- Operates over -40°C to 105°C

Ideal for use in portable, battery-powered applications in industrial, medical, and consumer designs

D/A Converter Family

Product	Resolution	Channels	Settling Time (typ)	Package
DAC081S101	8-bit	1	3 µsec	SOT-6, MSOP-8
DAC101S101	10-bit	1	5 µsec	SOT-6, MSOP-8
DAC121S101	12-bit	1	8 µsec	SOT-6, MSOP-8
DAC082S085	8-bit	2	3 µsec	MSOP-10, LLP-10
DAC102S085	10-bit	2	4.5 µsec	MSOP-10, LLP-10
DAC122S085	12-bit	2	6 µsec	MSOP-10, LLP-10
DAC084S085	8-bit	4	3 µsec	MSOP-10, LLP-10
DAC104S085	10-bit	4	4.5 µsec	MSOP-10, LLP-10
DAC124S085	12-bit	4	6 µsec	MSOP-10, LLP-10

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the current-limiting pin, ILIM, sets the input-current limit. The circuit contains all surface-mount components, and the high switching frequency allows the use of tiny inductors and capacitors, thus reducing total circuit size. You should use good PCB (printed-circuit-board)-layout practices.

The series-connected Polystor aerogel supercapacitors, available from various online sources, are each rated at 4.7F at 2.5V and feature a typical ESR (equivalent-series resistance) of 25 mΩ, thus allowing high discharge current. Low leakage current provides long capacitor-voltage-holdup time. The individual capacitor voltages track within 100 mV when charging and charge completely in less than 60 seconds at the rated charge current. **Figure 2** shows the capacitors' voltage, charge current, and resulting current drawn from the USB port when charging. **EDN**

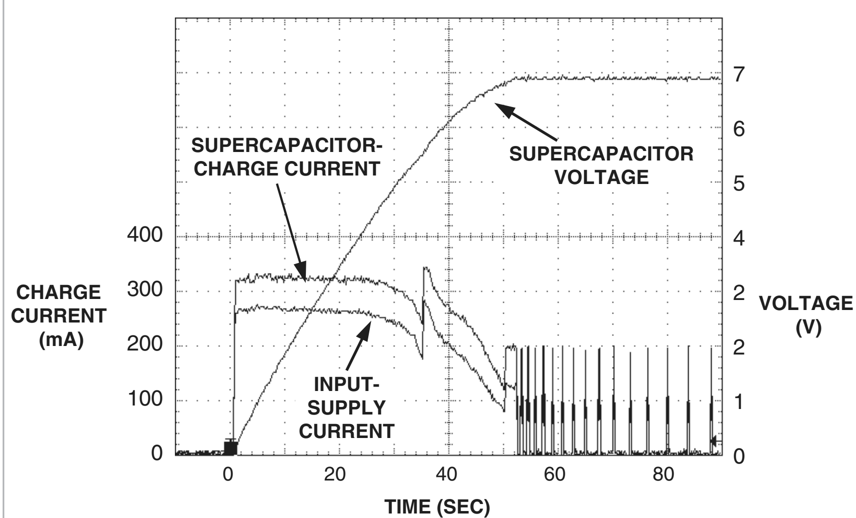
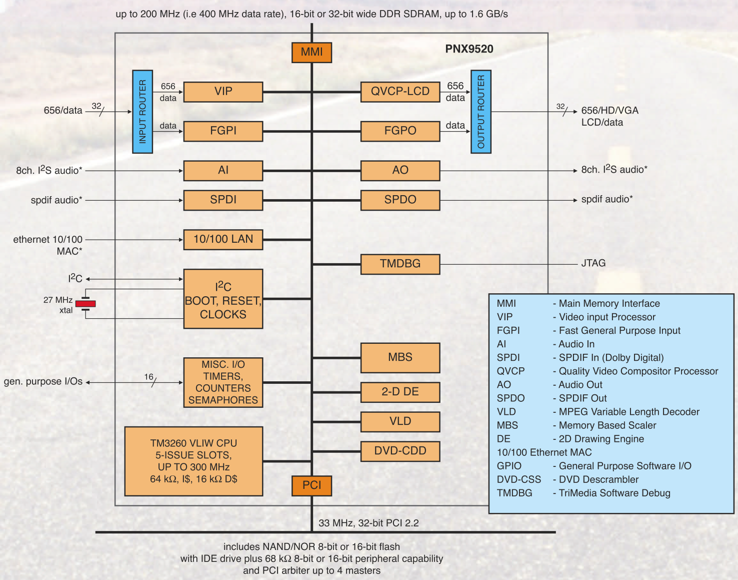


Figure 2 These curves show the super capacitors' voltage and charge current. Note that the charging current is 300 mA–the USB maximum allowable current draw.



PNX952x media processor family for automotive applications

The PNX952x family from NXP Semiconductors brings the flexibility and performance of Nexperia media processors to car infotainment. The family includes the only video processor you'll need, whether your system is handling video from DVD, digital TV, Flash media or connected devices – even two streams at the same time. Each one is packed with Nexperia technology to ensure a great picture for front seat and backseat occupants. They're as happy connecting to a mobile phone over Wi-Fi as to a media player over USB, and can even carry out high-end audio processing or digital terrestrial radio decoding. And they're also designed to keep up with developments as they take in-field software upgrades in their stride.

What if you could integrate in-vehicle media and digital radio technologies on a single chip?

NXP develops vibrant media technologies that help bring your ideas to life. Our innovative solutions enhance images, sharpen sound and simplify information sharing. Find out more about this highly integrated media processing solution for automotive infotainment on our website.

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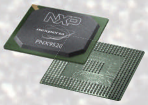
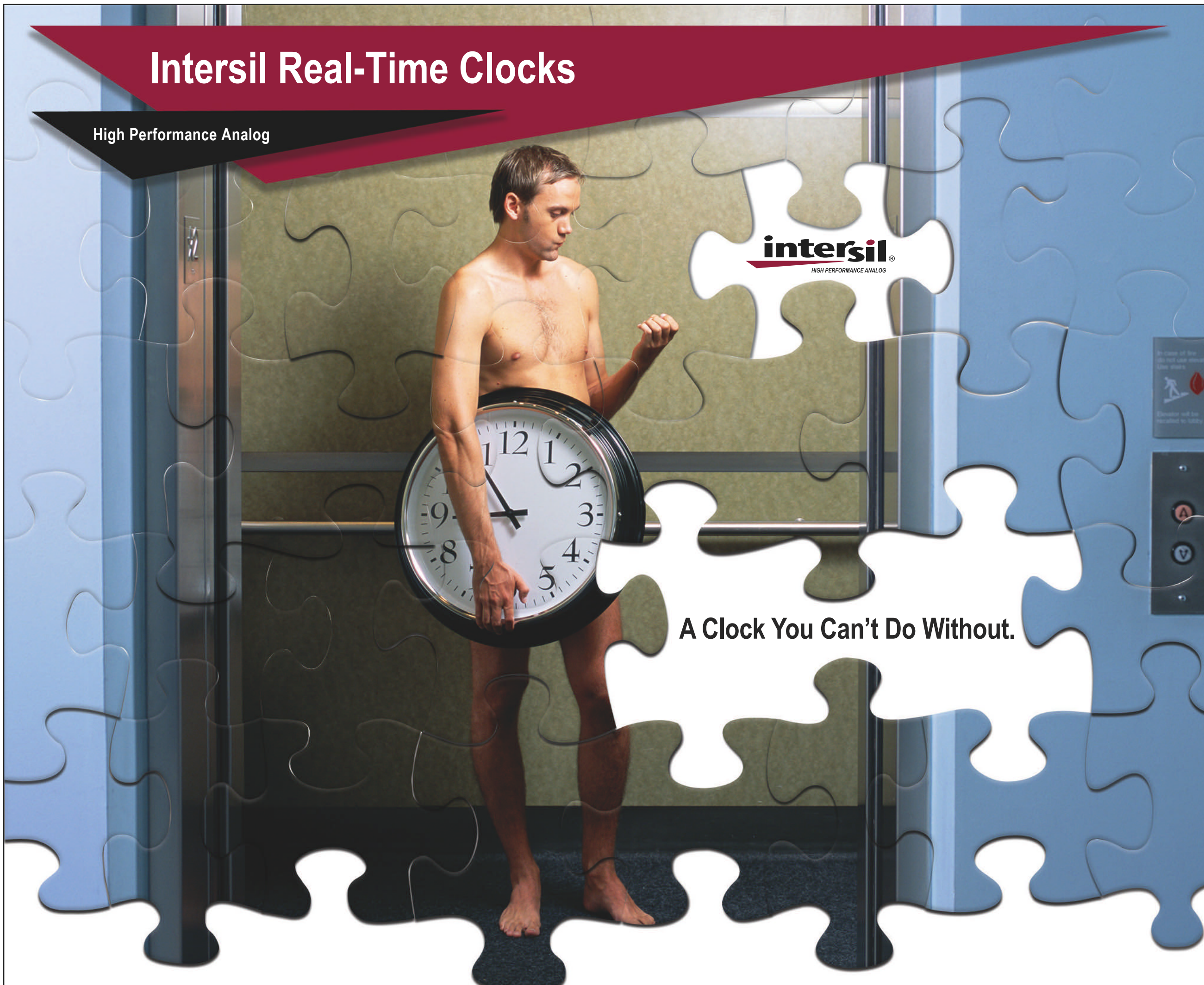
What if you could



NXP founded by Philips



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Automatic backup to battery or SuperCap

On-Chip Oscillator Compensation

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- 64-position digitally controlled trim capacitor
- Six digital frequency adjustment settings to ±30ppm

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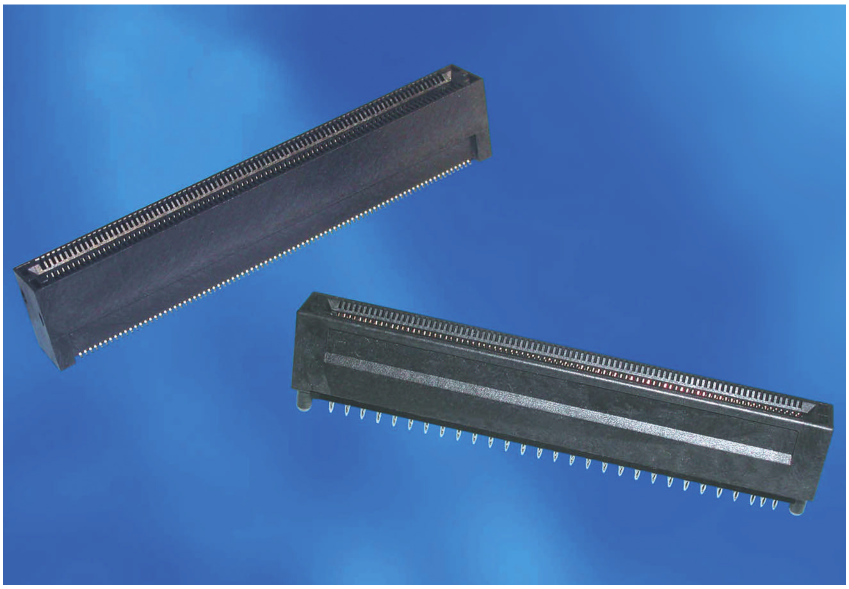
CONNECTORS



Card-edge connectors meet MicroTCA specifications

These press-fit card-edge connectors enable the use of MicroTCA architecture. Vertical connectors provide 170 contacts on 0.75-mm pitch and allow you to plug AMC cards into a backplane, providing speeds as high as 10 Gbps. The press-fit version extends the use of MicroTCA architecture to thicker backplanes that the standard surface-mount reflow-soldering process does not support. It targets larger and thicker backplanes, and the surface-mount connectors suit smaller and less complex backplanes. The MicroTCA connectors cost $9.60.

FCI, www.fciconnect.com

Connectors available with THR termination

Joining the vendor's D-subminiature connectors, vertical connectors feature THR (through-hole-reflow) termination. Processed within the SMT-manufacturing line, the reflow-capable THR connectors eliminate the need for wave-soldering, selective-soldering, and press-fit steps in production. Available with nine, 15, 25, or 37 pins, the male and female connectors measure 6, 6.3, and 9 mm, in accordance with DIN 41652 and CECC 75301-802. Creepage distance and clearance are 1.2 mm. The contacts are gold-plated in the mating area and tin-plated in the termination area. Available with a through-hole and a nut or a locking bolt, this locking hardware features antirotating protection and ESD-resistant premounting. The vertical THR D-subminiature connectors cost $1.

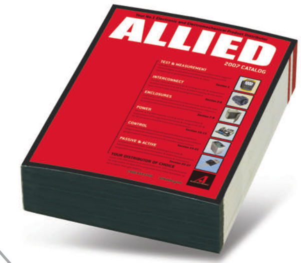
ERNI Electronics, www.erni.com

Plenum-rated cables have aluminum/polyester-foil shield

The 1325A two-pair and the 1326A three-pair STP (shielded-twisted-pair) Plenum-rated cables feature a smaller outside diameter and a low-smoke insulation and jacket. These low-capacitance cables are constructed with #22-AWG stranded, tinned-cop-

PHOENIX CONTACT





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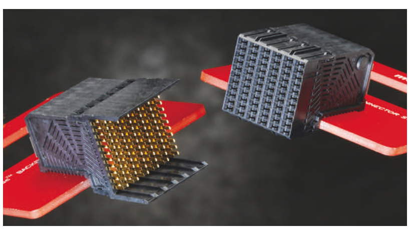
per conductors and a #24-AWG stranded, tinned-copper drain wire. The devices are NEC- and CEC CMP-rated. They employ the vendor's Beldfoil aluminum/polyester-foil shield, made using the Z-Fold isolation/shorting-fold construction. This process reduces potential noise ingress or egress by providing foil-to-foil contact where the shield's tape edges overlap. Available in 500- and 1000-foot lengths with white or blue jackets, the 1325A costs 39.4 cents per foot, and the 1326A costs 80.8 cents per foot.

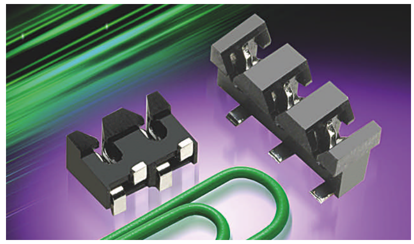
Belden, www.belden.com



Backplane-connector system suits standard and orthogonal architectures

For server, storage, telecommunications, and data-networking applications, the I-Trac backplane-connector system features a broadside-coupled, skew-equalized design able to handle 12.5 Gbps. The option to rotate the headers 90° on one side of the midplane allows the device to use the same part numbers for standard and orthogonal architectures. Support for quad-trace routing reduces PCB (printed-circuit-board)-layer count; you can reduce midplane PCB layers by leveraging the orthogonal capabilities of the device, which eliminate the need for PCB traces by using shared vias. The system consists of backplane-signal-header modules and daughtercard-signal modules. This system is available in seven-, 11-, and 15-row versions; an 11-row backplane-connector system costs 7 cents per mated line.

Molex, www.molex.com



Two- and three-position connector uses IDC technology

IDC (insulation-displacing-connector) technology allows the two- and three-position 9175 series connectors to attach individual wires to a single row of contacts. Features include a 1A continuous current rating at 25°C, a 125V voltage rating, a 100-MΩ minimum insulation resistance, and a 20-mΩ maximum termination resistance. The device has a −40 to +80°C temperature range. The connector's small footprint and ability to be quickly assembled make it suitable for high-volume applications in the consumer-electronics market. Available with a 2.45-mm profile, the 9175 Series costs 28 cents (10,000).

AVX Corp, www.avx.com

Press-fit contacts target mezzanine applications

Available in single- and double-row versions, devices in the STL unshrouded header-system family come in press-fit, dip-solder, and THR (through-hole-reflow)-termination types, as well as right-angle versions. The robust, permanent connection is vibration-resistant and insensitive to dirt and grime. Single-row unshrouded headers have a 50-pin count, and press-fit versions have a 36-pin count. Double-row unshrouded headers have a 100-pin count or a 72-pin count as a press-fit version. Connectors in this series measure 0.635×0.635 mm, and prices range from 15 to 30 cents each for a 10-pole STL.

ERNI Electronics, www.erni.com

INTEGRATED CIRCUITS

FM-radio transmitter combines receiver, transmitter into one chip

Able to receive an FM signal and transmit an FM signal to an FM tuner, the Si472x FM radio transceiver combines the functions of the vendor's Si470x FM radio receiver with the vendor's Si471x FM radio transmitter. The 3×3×0.55-mm chip compares with competing devices requiring at least two chips and five times more board space. Features include adjustable seek, soft mute, stereo blend, and an integrated antenna for receiving and transmitting. The Si4721 transceiver provides transmitter and receiver support for the European RDS (Radio Data System) and the US RBDS (Radio Broadcast Data System). The Si4720 costs $5.26 (10,000), the Si4721 costs $6.31 (10,000), and an evaluation board costs $150.

Silicon Laboratories, www.silabs.com

MIPI display buffer/controller simplifies mobile-phone design

The TC358730XBG high-speed MIPI (mobile-industry-processor-interface) display-buffer/controller simplifies the design of mobile phones and provides VGA-display resolutions. Features include 8 Mbits of embedded DRAM, single-buffer operation for images as high as VGA resolution, and automatic double buffering when handling two images with resolutions as high as HVGA. The device accepts high-speed, burst-access data transfers from the host, which enter the low-power sleep mode as the controller updates the connected LCD at the required frame rate, using low-leakage process technology, as well as sleep and deep-sleep modes. Image-processing functions include pixel-doubling to scale lower resolution images to higher resolution displays, rotation of incoming images, and the mirroring of incoming and outgoing images. The vendor's Magic Square algorithm provides image-quality-enhancement capabilities, allowing an RGB666 18-bit LCD panel to produce picture quality equivalent to an RGB888 24-bit LCD panel with as many as 16 million colors. The buffer/controller supports three host-interface standards, a primary LCD, and a secondary LCD through DBI Type C. The device provides 1.8V for the I/O, 2.3 to 2.9V for the embedded DRAM, 1.2V for the internal-core operation, and 1.8V for the external-core operation. Measuring 5×5×1 mm in a BGA-64 package, the TC358730XBG is available for $20 to $25 (10,000).

Toshiba America Electronic Components, www.toshiba.com

Zero-drift, programmable amplifier reduces input noise

The zero-drift, 5-μV-typical-offset AD8231 digitally programmable-gain instrumentation amplifier provides 80% input-noise reduction compared with competing devices. A three-op-amp instrumentation architecture allows a 50-nV/°C voltage-offset drift. Features include rail-to-rail inputs and outputs at 1-MHz bandwidth, 10-GΩ inputs, a −40 to +125°C temperature range, a 122-dB CMR (common-mode rejection), and an additional on-chip op amp. Operating on a 3.3 to 5V supply, the device draws 3.5-mA supply current with 1-μA supply current. Asserting the shutdown pin reduces the supply current to 1 μA. The amplifier's programmable gains are one, two, four, eight, 16, 32, 64, and 128. Manufactured using the iCMOS (industrial-CMOS) process allows for a 32-nV/$\sqrt{Hz}$ input noise. The package has a wide center panel to keep the part securely soldered to the PCB (printed-circuit board) in high-vibration environments. Available in an LFCSP-16 lead package, the AD8231 costs $1.69 (1000).

Analog Devices, www.analog.com

INTEGRATED CIRCUITS

Cable-extender chip set enables data transfers over 400m cables

Using SiGe (silicon-germanium) BiCMOS-8 process technology, the low-power DS15BA101 and DS15EA101 cable-extender chip set extends serial-data streams from serializer/deserializer and FPGAs over Category 5 and coaxial cable at half the cost of fiber-optic devices, claims the vendor. The chip set increases the reach of 0.15- to 1.5-Gbps LVDS (low-voltage-differential-signaling), LVPECL (low-voltage-positive-emitter-coupled-logic), and CML (common-mode-logic) signals to 400m over copper cable with 360-mW power consumption. The DriveCable002EVK reference design supports Category 5, 5e, 6, and 7 100Ω twisted-pair cables as long as 100m and 50Ω coaxial cables as long as 400m. Available in a 3×3-mm LLP-8 package, the DS15BA101 differential buffer has a 3.3V power supply and consumes 150 mW at 1.5 Gbps; the DS15EA101 adaptive equalizer comes in a 4×4-mm LLP-16 package, has a 3.3V power supply, and consumes 210 mW at 1.5 Gbps. The DS-15BA101 cable driver also functions for level-translation between LVDS/CML/LVPECL and CML or LVPECL. The DS-15BA101 and DS15EA101 cost $4 and $8.75 (1000), respectively.

National Semiconductor, www.nsc.com

EMBEDDED SYSTEMS

100W servo-motor controller suits brush motors with quadrature encoders

Targeting brush motors running at less than 100W with quadrature encoders, the 3C20 digital-motion controller claims a 32-bit or greater precision in position, velocity and acceleration, and jerk parameters. This DSP-based, single-axis dc servo-motor controller/amplifier features a 30-MIPS, 16-bit DSP and a 100W H bridge. The device has a trapezoidal-profile capability and provides time-based S-curve profiles with a sequence of jerk values and delay tokens in the FIFOs. Measuring 2×2 in., the 3C20 digital-motion controller costs $54 (100).

Mesa Electronics, www.mesanet.com

Telephone-interface module is half the size of its predecessor

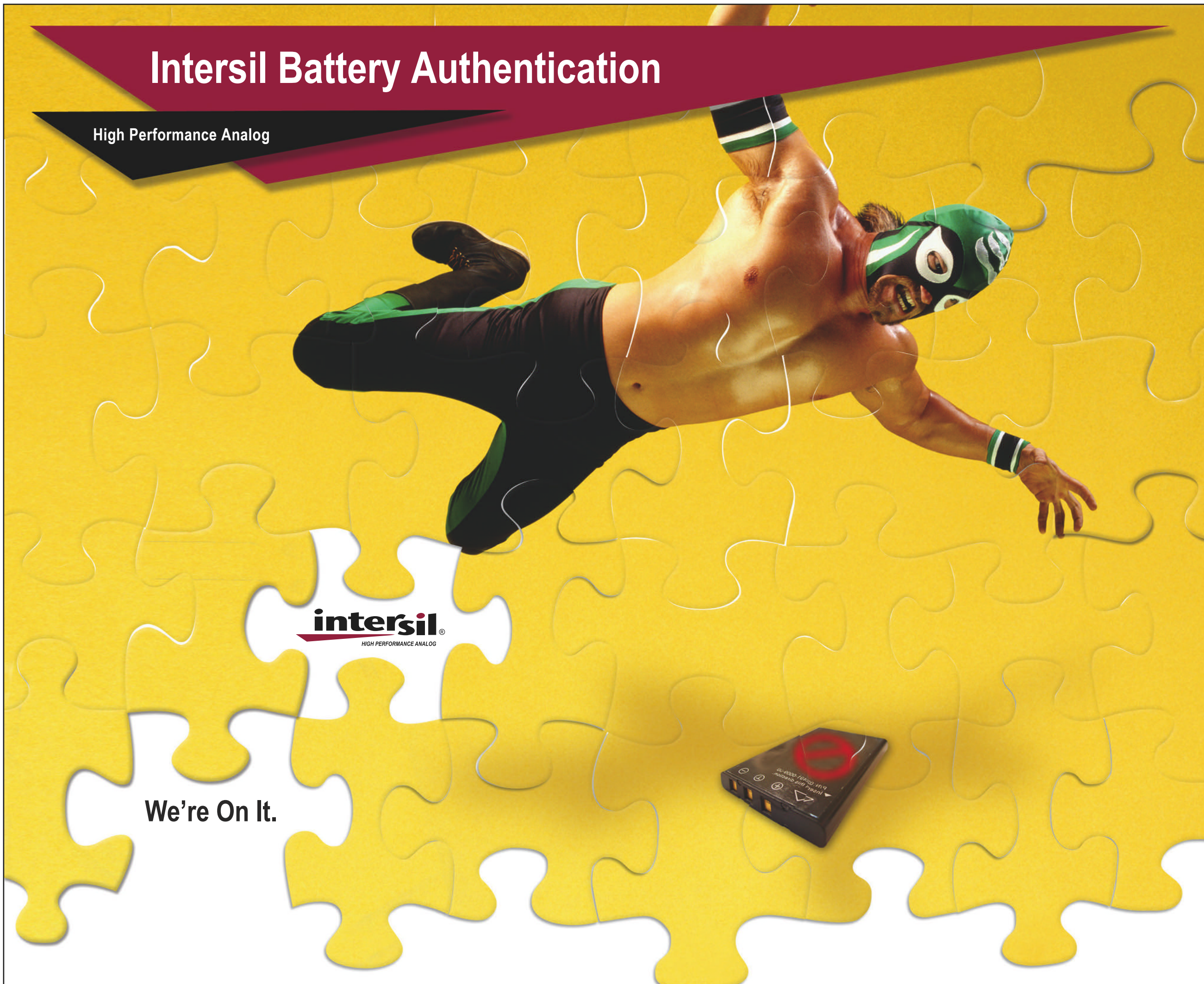
Measuring 0.8×0.78 in., the XE-0402LCC telephone-interface module is half the size of the previous-generation device. Features include a solid-state hook switch, caller-ID pass-through, and a ring detector. The module also provides a 3000V-ac isolation barrier. The device supports a dial-back-up feature for VOIP systems, audio and data transfer for security applications, and an audio bridge for radio systems. The XE0402LCC costs $6.30 (5000).

Xecom, www.xecom.com

Module supports CRT/LVDS

Targeting small embedded systems, the MB-09014 Ext microprocessor module has a 114×94-mm form factor. Features include an onboard 600-MHz, 512-kbyte Intel Celeron processor, an LVDS (low-voltage-differential-signaling) CRT, a 10/100-Mbps Ethernet interface, and support for AC'97 audio. System drivers are available for Microsoft Windows XP/XPe/CE and Linux. The device includes a DDR SO-DIMM socket providing 1-Gbyte, 266-MHz support. The MB-09014 Ext costs $276.

Win Enterprises, www.win-ent.com



Intersil's **ISL9206 FlexiHash+™ Engine delivers high-security battery authentication** at a low cost.

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ISL9206 Key Features:

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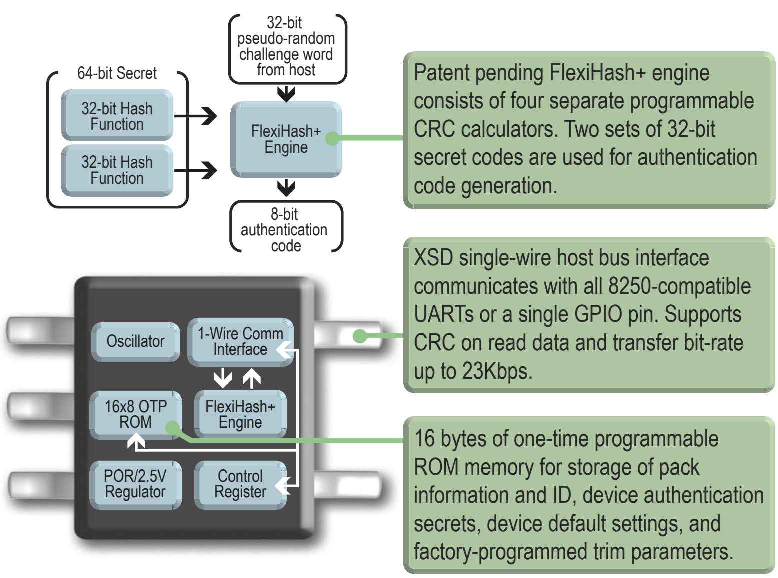
- FlexiHash+ engine uses two sets of 32-bit secrets for authentication code generation.
- 16x8 one-time programmable ROM memory.
- Additional programmable memory for storage.



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LOOKING AHEAD

TO IITC 2007

The 10th annual IEEE IITC (International Interconnect Technology Conference) kicks off on June 4 in Burlingame, CA. The premier technical conference for engineers developing on-chip interconnect technology, IITC started the year after IBM changed the interconnect world with the introduction of its copper-damascene process, transforming interconnect from just a way to hook transistors together into the enabling technology element it is today. This year, the conference will look back at the impact of that seminal revolution and look forward to the technologies that have a similar potential for tomorrow's chips: among other things, 3-D ICs, the use of carbon nanotubes as practical on-chip interconnect, high-speed noncontacting interconnects, multiple-air-gap structures, and self-forming dielectric barriers in the interconnect stack.

LOOKING BACK

AT THE MARCH OF MINIATURIZATION

Rapid changes will continue in the trend toward microminiaturization, in the view of HA Stone, Jr, of Bell Laboratories. For the next four or five years, these changes will occur at an increased rate in such areas as digital computers and telephone central-office equipment. Progress will reduce resistors and capacitors to a tenth or even a hundredth of their physical size today. Inductors and transformers will not shrink to this degree, although substantial progress will occur. This will require advanced packaging concepts. In addition, microminiaturization will require driving up the reliability of these components to one failure in 1 million parts, and it will require automated assembly techniques to preserve these reliability figures.—*Electrical Design News*, April 1957

LOOKING AROUND

AT THE RISING CLEAN-ENERGY TIDE

Whatever you may think of global warming, there is no question that carbon-light and renewable energy sources and energy conservation have surged in popularity. On the surface, this information should be great news for the electronics industry. Most non-fossil-fuel power-generation schemes are relatively smaller and heavy in electronics content. And energy conservation begins with embedded intelligence. But two observations in recent weeks are more worrying. First, analysts are reporting that the demand for solar cells is beginning to squeeze wafer supplies, threatening cost structures for ICs. A second report warns that the energy craze is beginning to attract a flood of venture funding, potentially at the expense of early-round funds for electronics, EDA, and software ventures. There's no predicting the outcome on this one.